

FPGA Mezzanine Cards for CERN's Accelerator Control System

Plus some reflections on Open Hardware

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BE-CO Hardware and Timing section
CERN

ICALEPCS 2009



Outline

- 1 Introduction
- 2 The FMC standard
- 3 CERN's implementation
- 4 Open Hardware



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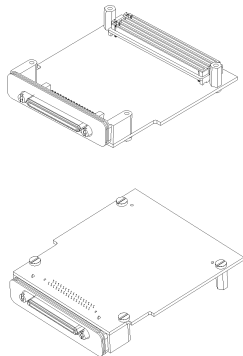
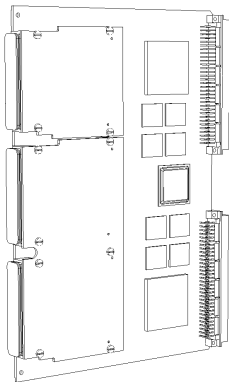


Background

- CERN's BE Controls group supports a kit of standard hardware modules.
- Support includes stocks management, help in debugging and low level software:
 - Linux Device Drivers.
 - C/C++ libraries with usage examples.
 - Test programs for drivers and libraries.
- With the injectors renovation project, supported platforms will include PCI and PCIe in addition to VME.
- A carrier/mezzanine strategy has been adopted.



Carrier/mezzanine approach



Courtesy of VITA: <http://www.vita.com/fmc.html>

Advantages of the carrier/mezzanine approach

Re-use

One mezzanine can be used in VME, PCI and PCIe carriers.

Reactivity

No need to place and route a complex FPGA PCB for every new user need.

Rational split of work

Controls can design the carrier, Instrumentation an ADC mezzanine, RF a DDS one, etc.

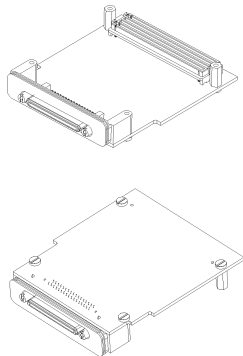
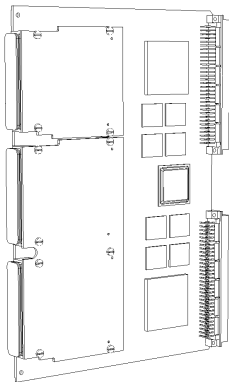


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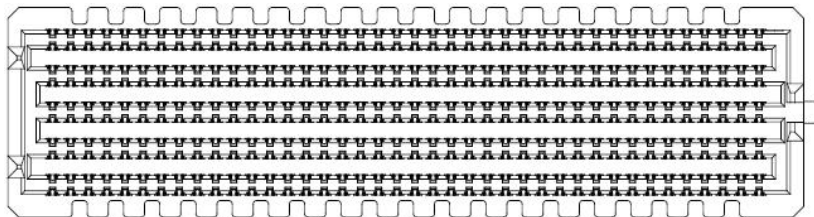


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Courtesy of VITA: <http://www.vita.com/fmc.html>

Connectors



- Ball Grid Array (BGA) characterized for high bandwidth applications.
- Low Pin Count (LPC) and High Pin Count (HPC) variants with 160 and 400 contacts respectively.



Agnosticism

- Pin function, sense – input or output – and electrical standard are defined at FPGA configuration time.
- Carrier reads FMC identity through an I2C serial bus and configures the FPGA accordingly.



Physical Dimensions

- Small dimensions for thermal reasons.
- Keep all digital circuitry in the carrier.
- Use FMC for front panel connectors and analog.

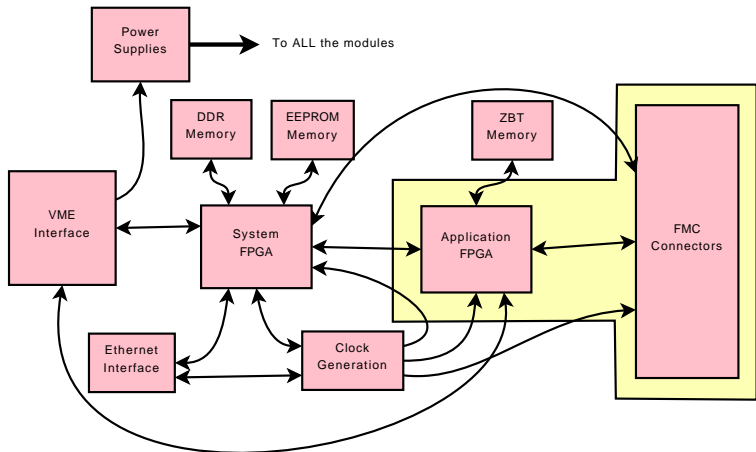


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Carrier design



Ongoing developments

Carriers with timing (White Rabbit) support

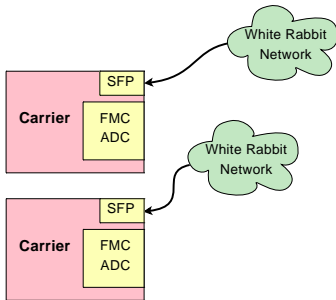
- VME with two single-width (one double-width) slots.
- PCIe with one single-width slot.

Mezzanines

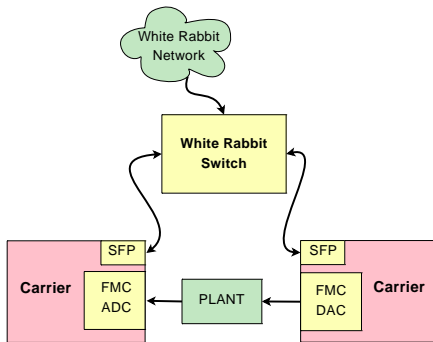
- Two-channel 100 Ms/s ADC with oscilloscope-type analog front end.
- Four-channel 10 Ms/s programmable Analog Waveform Generator.



Use cases



Distributed oscilloscope



Distributed feedback system



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Advantages

Peer review

Get your design reviewed by experts all around the world, including companies!

Design re-use

How many people are designing a 100 Ms/s ADC independently, making the same – or different – mistakes?



Role of companies

Design partners

Pay a company specialized in a given topic to design a specific card with/for you.

Commercial partners

Buy the cards you designed from a company that will take the charge of manufacturing, testing, managing stocks and providing support.



Open Hardware Repository: <http://www.ohwr.org>

A very useful tool

CERN BE-CO-HT and Cosylab teamed up to build a web-based collaborative tool for electronics designers.

Made itself of open software

- Twiki.
- Mailman.
- SVN.
- Bugzilla.



Summary

- The first **agnostic standard** to interface mezzanines and FPGAs.
- We will adopt it to **improve support** of hardware and **reduce maintenance** costs.
- Combined with Open Hardware paradigm and collaborations, it can **reduce duplication** and **improve design quality**.
- Outlook
 - Finish carrier design before end 2009.
 - Start collaboration with companies for series production of carrier and ADC/DAC FMCs.

