Development of a New Phase Detector for the APS Linac

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Abstract

An effort is being made to upgrade the Advanced Photon Source linac radio frequency (rf) phase detector system. The decision was made to replace the current phase measurement system, which is based on a Los Alamos National Laboratory designed analog vector detector module, with a digital I/Q method. As an initial step we reconfigured one of our current 8-channel, 14-bit ADC designs, originally developed for the storage ring beam position monitor system, to perform the I/Q sampling and the phase and magnitude computations. This paper discusses the current board design, proposed modifications to optimize the board for this application, and field programmable gate array design.

Background

The BPM data acquisition board, shown in figure 1, consists of eight Analog Devices [3] AD6645, 105MSPS ADCs, an Altera© [2] Stratix II FPGA and a Arcturus Networks [4] uC5282 microprocessor module, which acts as the input/output controller (IOC) processor. The flexibility of the FPGA allowed us to easily modify the design to create a phase measurement board, employing I/Q sampling techniques. The board also has 12 digital TTL outputs, several trigger inputs (SMA and SMB) for synchronization, a reference clock input and two fiber signals that are currently configured to interface event signals from the APS event system.

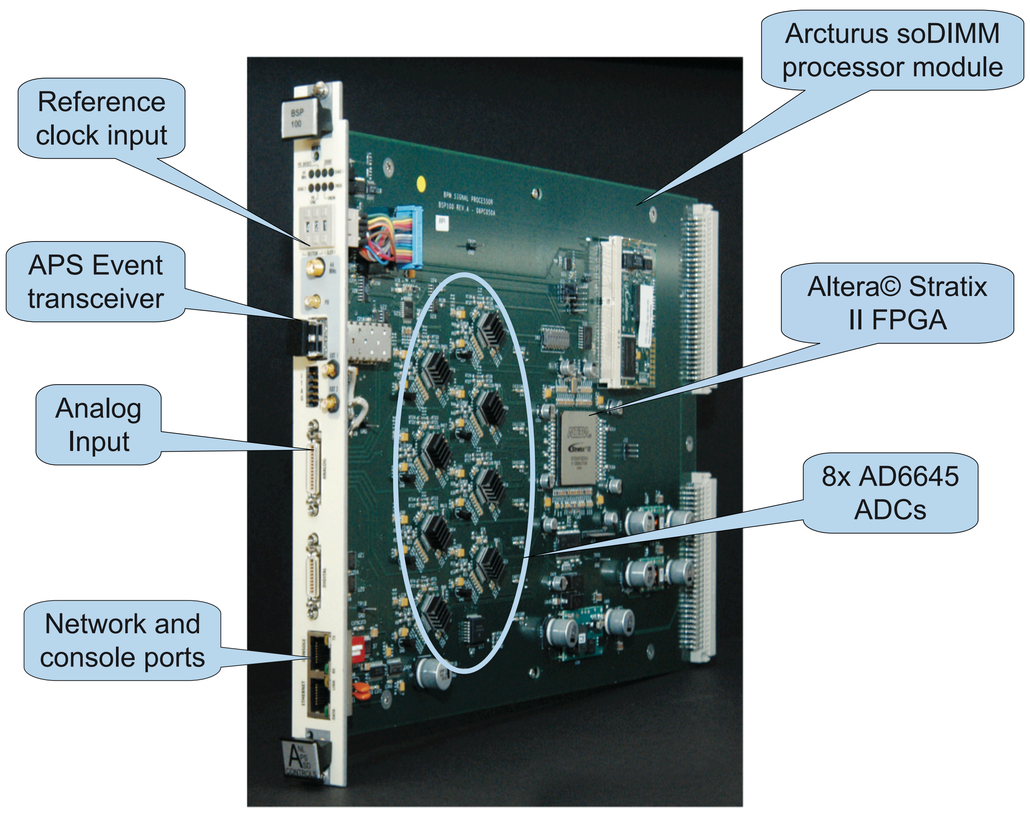

Fig. 1. BSP100 - BPM signal processing board used for the phase detector prototype

Prototype Shortcomings and Adaptations

- Awkward front panel connectors.
  - Used a breakout panel with isolated BNC connectors.
- Inconvenient external reference and external trigger signal levels.
  - Used a custom VME board which converts rf signals to LVTTL signals.

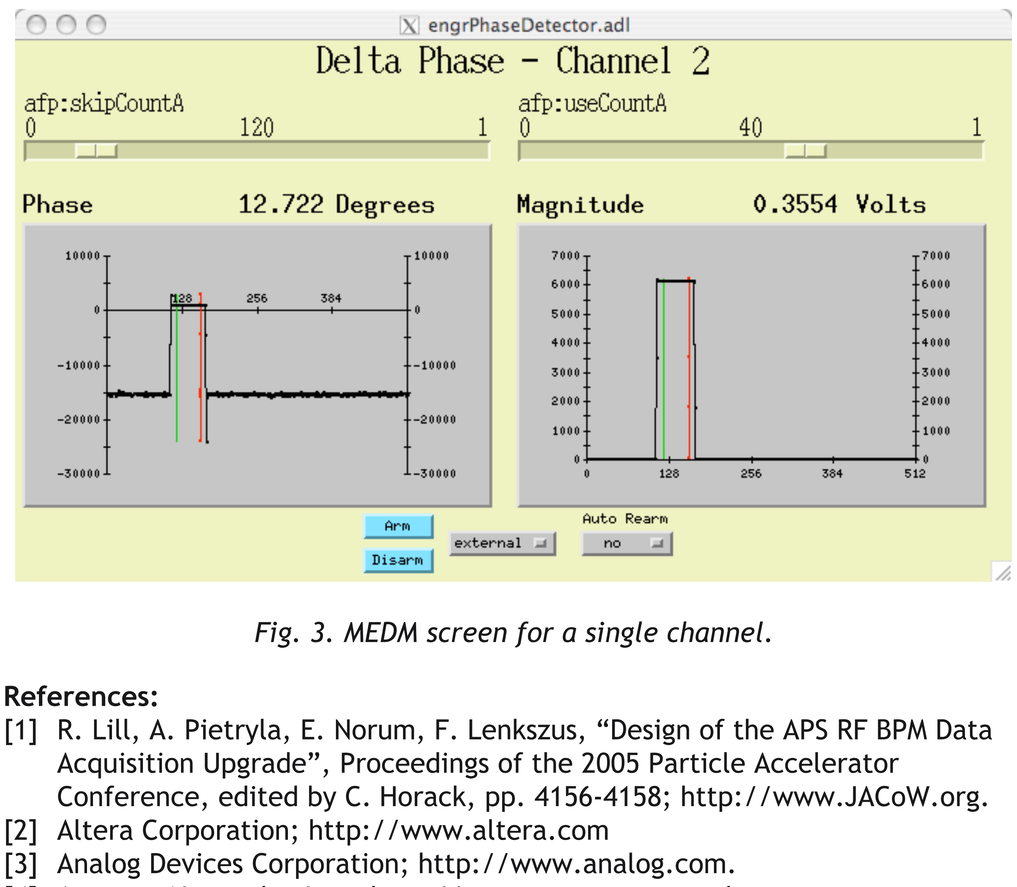

Fig. 3. MEDM screen for a single channel.

References:

[1] R. Lill, A. Pietryla, E. Norum, F. Lenkszus, “Design of the APS RF BPM Data Acquisition Upgrade”, Proceedings of the 2005 Particle Accelerator Conference, edited by C. Horack, pp. 4156-4158; http://www.JACoW.org.
[2] Altera Corporation; http://www.altera.com
[3] Analog Devices Corporation; http://www.analog.com.
[4] Arcturus Networks, Inc.; http://www.arcturusnetworks.com.
[5] 3M Company; http://www.3m.com/index.html.
[6] Andrew Corporation; http://www.commscope.com/andrew/eng/index.html.

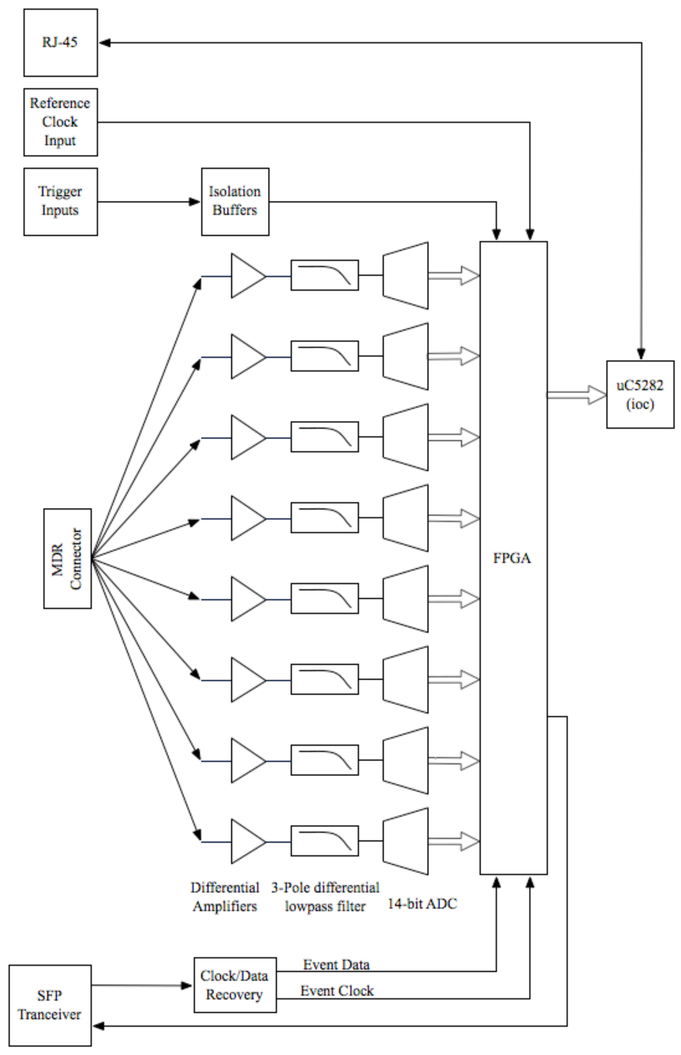

Fig. 2. Simplified board level block diagram

FPGA Design

- Accepts 20MHz reference signal synchronous to the down-converted linac rf.
- Multiplies reference clock by 4x to 80MHz via PLL.
- All ADCs clocked synchronously.
- All I/Q and phase/magnitude processing performed synchronous with reference signal.
- Waveform and average signals can be triggered either via an external trigger or via the APS event system.
- “Region of interest” measurement capability.

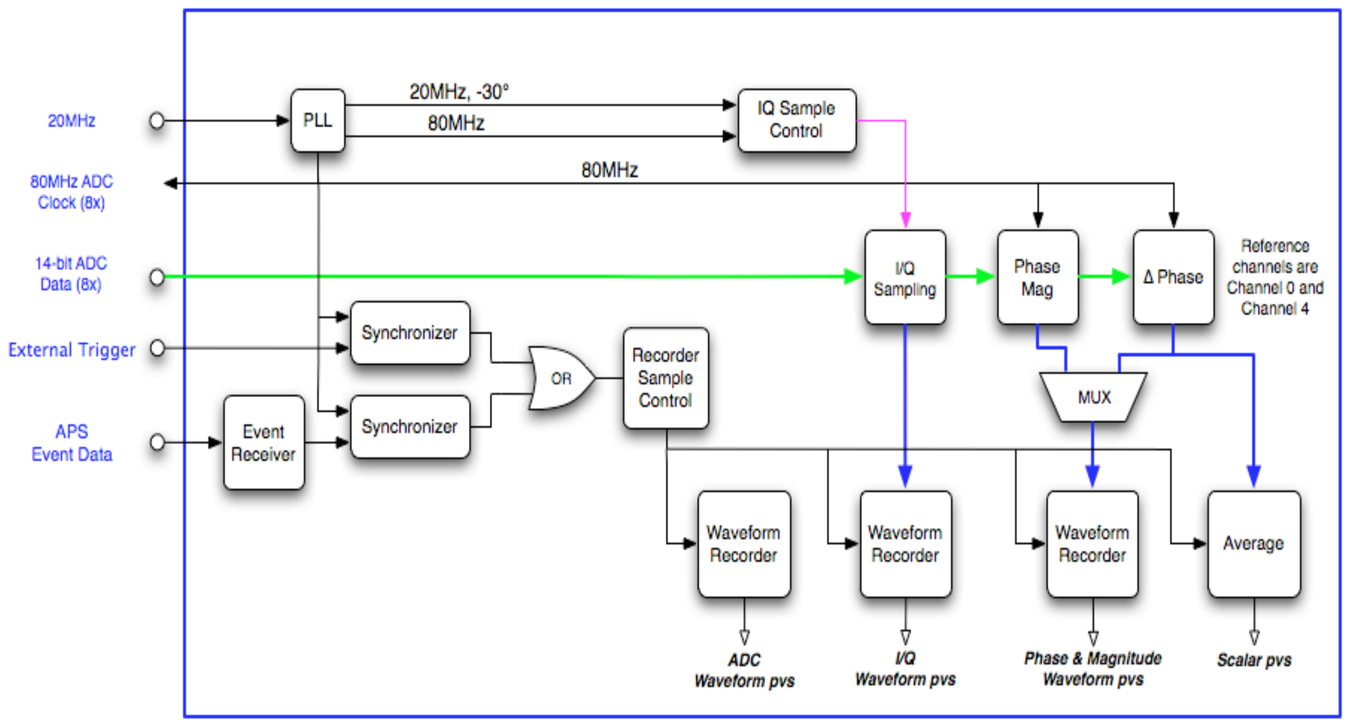

Fig. 4. Block diagram of the FPGA

Preliminary evaluation has demonstrated a system noise floor of 0.012° rms using 1 sample per measurement. With 40 samples per measurement, 2 μs of data, the noise floor is reduced to 0.005° rms.

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