The Control System of the ATLAS Pixel Detector

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The innermost part of the ATLAS experiment is a pixel detector, built of 1744 individual detector modules. To operate the modules, readout electronics and other detector components a complex power supply and control system is necessary. While the hardware is mainly built by units which are specially adapted to the needs of the pixel detector, the control software has to support these special needs, while in parallel it is embedded into the ATLAS wide control system. Core of the pixel detector control is a PVSS based SCADA system in combination with a finite state machine. An overview on the pixel detector hardware and a report on the commissioning of the final control system will be given. We concentrate on the description of the finite state machine and its interaction with several additional protection routines.

The ATLAS Pixel Detector

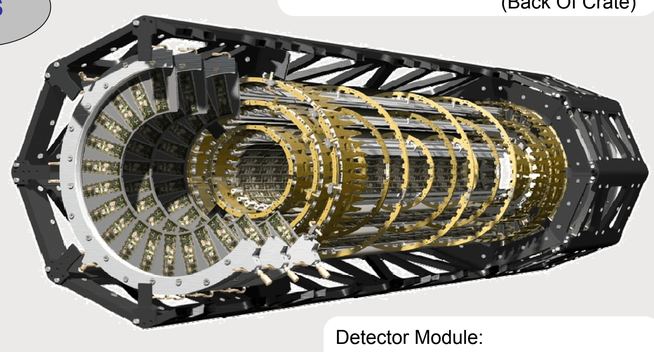
Mechanics:

length: 1.3 m, ∅ 34.4 cm, weight: ~4.4 kg
112 staves are mounted on 3 shells
3 disks in each endcap
disk sectors and staves: **1744 detector modules**

Optical data transfer:

272 readout groups
on-detector opto-transceiver: optoboard
off-detector opto-transceiver: BOC card (Back Of Crate)

DCS



Detector Module:

Silicon based sensor, 46080 pixels
16 front end readout chips
1 module control chip

88 Parallel Cooling Circuits/loops:

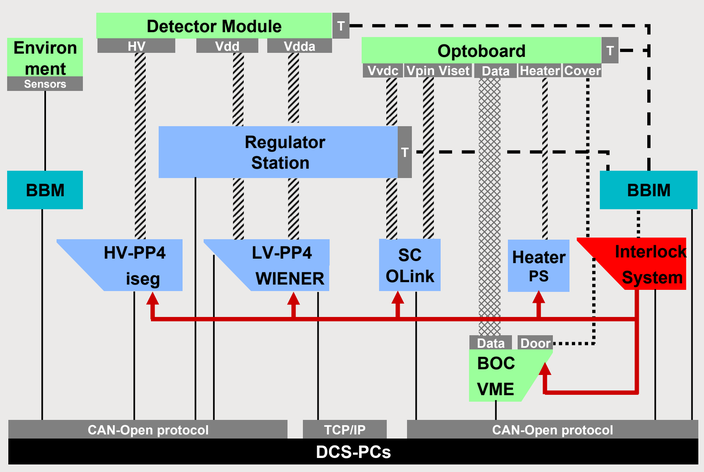
56 PCCs with 2 staves each
24 PCCs with 2 disk sectors each
8 PCCs for 272 optoboards

80 million readout channels

Pixel DCS Hardware

The DCS hardware supervises detector modules, the optoboards, the readout crates, and the environment. It consists of:

- The power supply system (iseg HV, WIENER LV, regulator station, Supply and Control of the OptoLink, and PS for the Optoheaters)
- Monitoring units (Building Block Monitoring, respectively Building Block Interlock and Monitoring)
- The interlock system



The DCS Software

PVSS II (by ETM, Eisenstadt, Austria) was selected by the LHC experiments' Joint Controls Project (JCOP) as a base for the individual control systems.

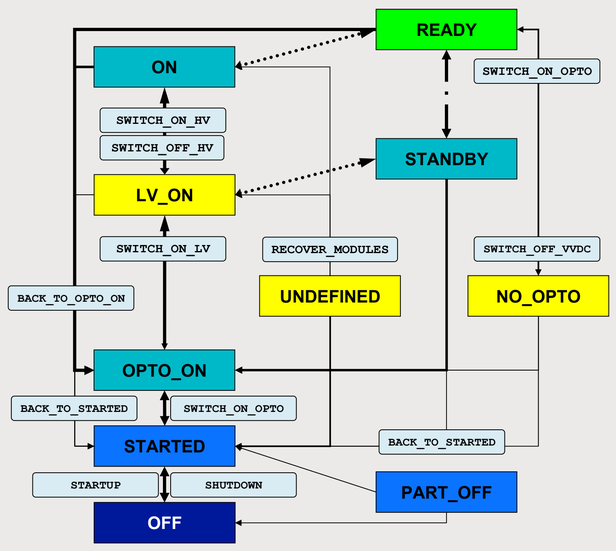
Pixel DCS is built of 3 software layers:

- Frontend Integration Tools (FIT):
  - Establish communication to the hardware
  - Data structures follow hardware properties
- System Integration Tool (SIT):
  - Mapping between hardware and detector
  - Initialises archiving of DCS data
- Finite State Machine (FSM):
  - Tools are provided by JCOP framework and ATLAS DCS
  - Overview of detector via hierarchy of FSM objects and their states
  - Commands allow for a change of the operation mode
  - Operation of detector

Readout Group: State Diagram

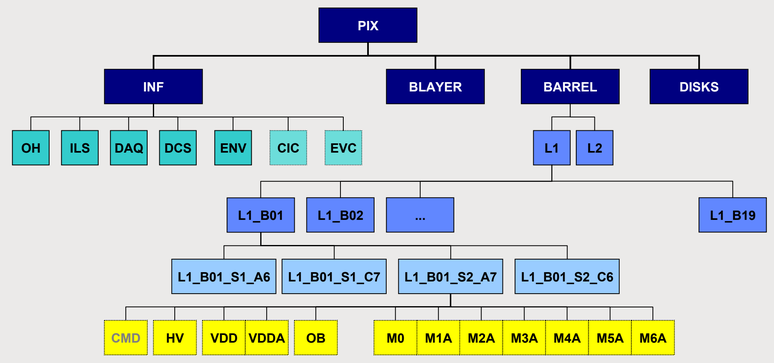
The operation of the pixel detector is based on the control of the readout groups, and the implemented states reflect on its special operational aspects.

- OFF is the state which corresponds to a complete shutdown
- With the startup command, the hardware is brought into a defined, STARTED state, but there is still no power on-detector.
- The optoboards can be switched on as soon as the corresponding cooling loops are operated. The OPTO_ON state is reached when the optoboards are fully powered and the off-detector lasers are on.
- The modules must only be powered when the lasers are on. The transition to LV_ON is allowed when the optoboards are ready and the corresponding cooling loops are on.
- HV must stay off during unstable beam conditions. This dedicated safe state is called STANDBY.
- When the readout group is ON (HV on), the modules must still be configured by the DAQ in order to be READY for data taking.



The Pixel FSM Tree

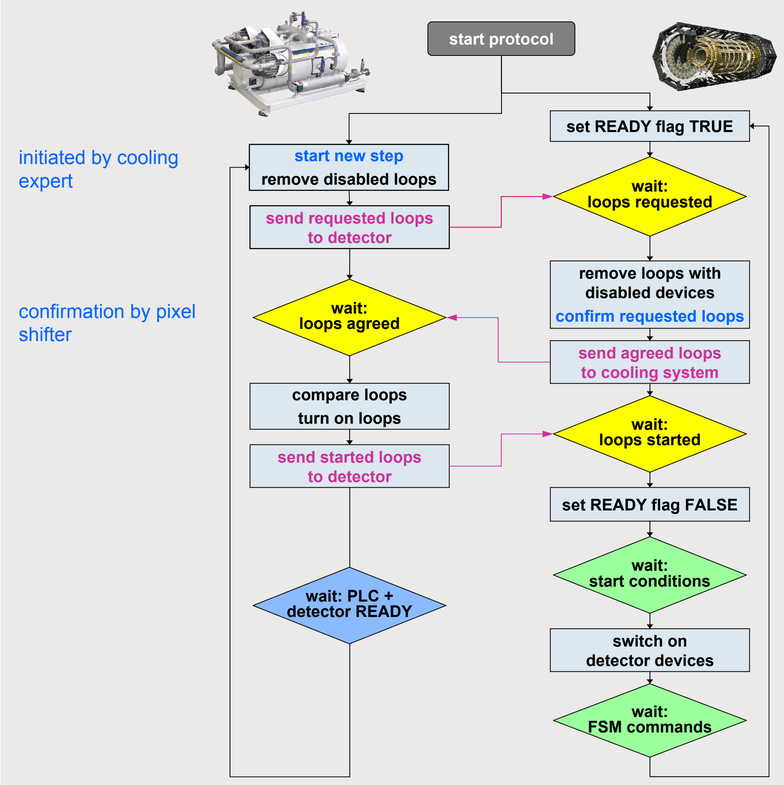
- The subdetector node, PIX, is composed of the DAQ partitions and the infrastructure (ATLAS requirement).
- The tree follows the mechanical structure of the detector, i.e. shells and cooling circuits.
- The readout groups are the smallest units concerning common services.
- At the lowest level the Device Units transform hardware information into states and synchronize commands to the corresponding device channels.



Handshake with Cooling

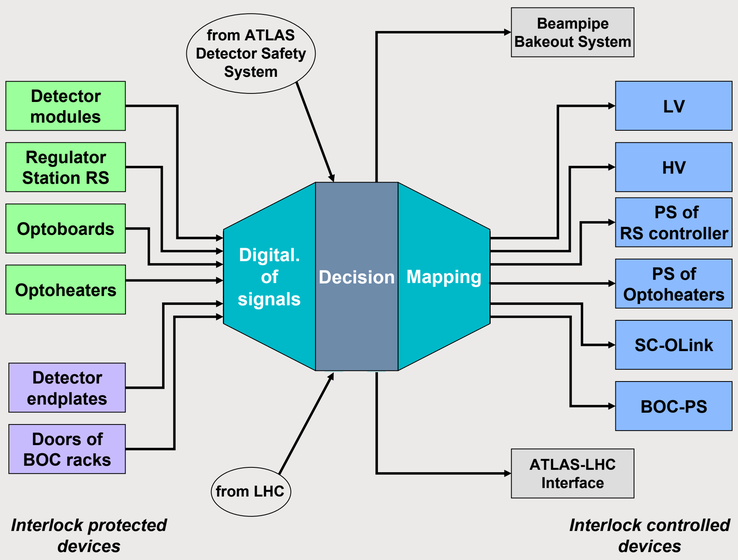
The operation of pixel detector and cooling system is strongly depending on each other: The pixel detector must be protected against overheating, while the cooling system requires a stable heat load.

To guarantee a fast and efficient common startup, a semi-automatic handshake protocol has been established.



The Interlock System

- The interlock system protects all equipment (detector modules, optoboards, optoheaters, and regulator stations) against overheating.
- Human beings must be protected against risks due to infrared lasers (located close to the detector endplates and in the BOC crates).
- The Interlock Matrix determines which devices have to be switched off and maps the signals to the corresponding power supply channels.



The User Interface for the Finite State Machine

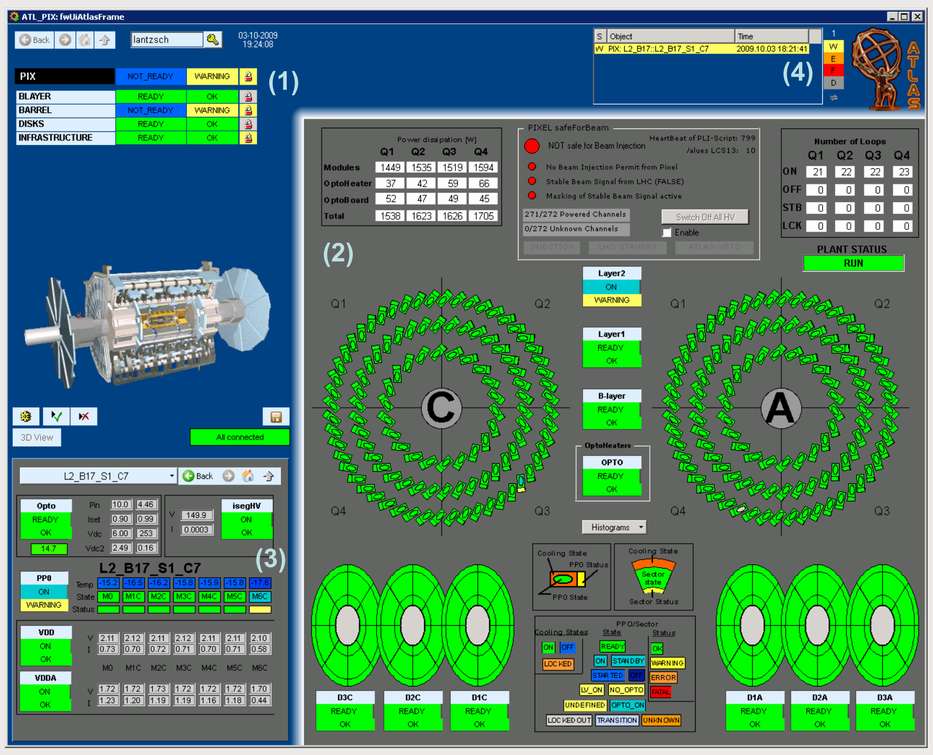
The pixel specific panels are embedded in the ATLAS FSM, and so the GUI shares the common structure:

(1) Display of state (operation mode) and status (“health”). Sending of user defined commands.

(2) Main panel for the selected node. Defined by the subdetectors.

(3) Secondary panel, allows monitoring of chosen node while navigating elsewhere.

(4) Upcoming error conditions can be tracked.



The main pixel subdetector panel provides the operator with the information needed for effective supervision and operation.
It grants a complete overview by displaying for all 272 readout groups

- state
- status
- information on cooling loops

and allows fast navigation in main and secondary panel to the level where the actual hardware information can be checked.

During commissioning, calibration, and cosmic data taking, the FSM has proven to be an adequate tool for the operation of the pixel detector.