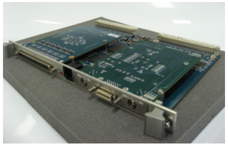
Applications and Upgrade of Flexible and Logic-reconfigurable VME Board

T. Hirono, T. Ohata, and T. Kudo

JASRI/SPring-8, Sayo, Hyogo 679-5198, Japan

1. Introduction

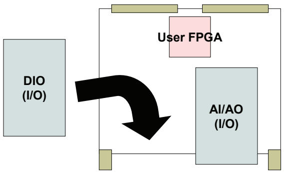
We developed a flexible logic-reconfigurable VME board*.



It can be used in a wide range of application, for which rast fast(20ns～) and real-time control must be achieved.

The VME board has two components: a base board and I/O mezzanine cards.
•The base board has a FPGA for user to reconfigure and execute their sequences.
•The I/O cards are mounted on base board with connectors and screws.

*T. Hirono, T. Ohata, and T. Kudo,
"Developments of the flexible and logic-reconfiguable VME board"
Proc. of ICALEPCS 2007, Knoxville, U.S.A., (2007)



However,

- When you apply the flexible and logic-recofigurable VME board to your system, you need to….
  1) select appropriate I/O mezzanine cards.
  (or develop a simple mezzanine card with required I/O speculation)
  → Easy !
  2) develop a firmware of FPGA.
  → Time consuming… → The board was not applied because of limited developing time
- External data bus is VME-bus only.
  → Too slow for many of data acquisition system…→The board was not applied

➡ **We created a novel development environment for the VME board to shorten development period**

➡ **We upgraded the base-board to enable fast and massive data transfer.**

2. Development Environment

Requirements and its solutions for a development environment

1) Implementation Language

Implementation language required to be familiar to the users.
→ We adopted C because the major control system in SPring8 are developed in C.

2) Ability to support various I/O mezzanine cards

We have 4 types of I/O mezzanine cards, and more in the future. The development environment required to support all these I/O mezzanine cards.
→ We adopted is ImpulseC and synthesis tools provided from Xilinx as compilers.

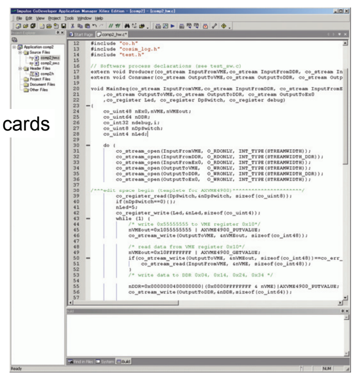
3) Separation of codes

Codes unrelated to the user's algorithm required to be separated from a codes of the user's algorithm.
→ We developed data transfer sequence in VHDL.

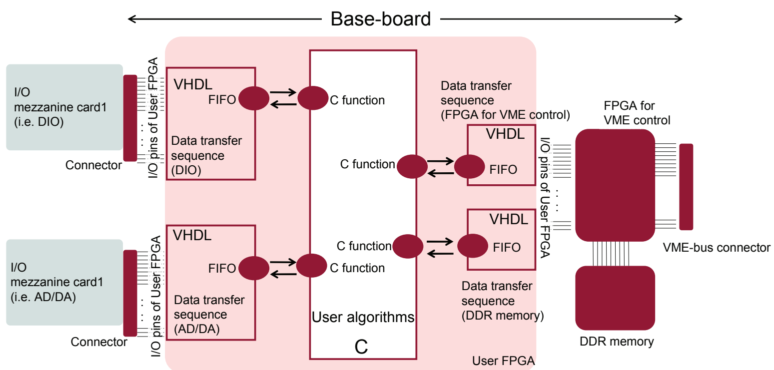
4) Simple compiling

Compiling procedure required to be simple.
→ We developed TCL script and bat files. The compiling was done by a single "build" button on Impulse C editor.

A screenshot of ImpulseC editor



A Block diagram of the firmware with devices accessed from the user FPGA.

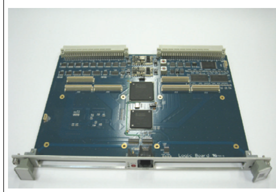


3. Upgrade of Base Board**

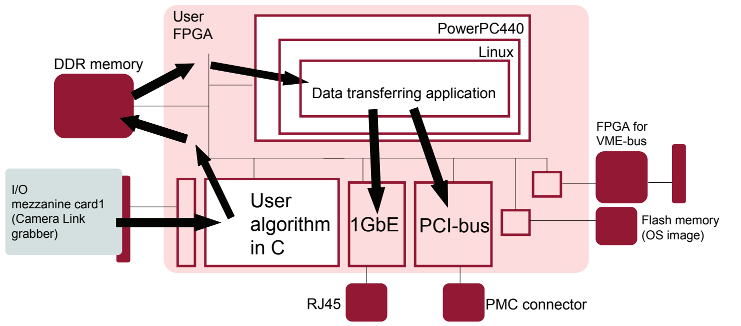
**The new base board was developed in cooperation with ARKUS Inc.

Gigabit Ethernet port and PCI mezzanine card interface was equipped on a new advanced base board to support massive and fast data transfer. Linux runs on the user FPGA and controls 1G Ethernet and PMC.

Specification of the new advanced base board and the existing basic base board.

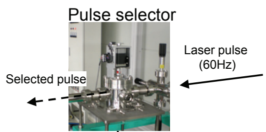
	Advanced base board (NEW!)	Basic base board
		
User FPGA	Xilinx Vertex5 XC5VFX70T	Xilinx Spartan3 XC3S1500
Bus	VME revision C.3	VME revision C.3
Memory	512 MB DDR, 8MB Flash, SD card Socket	256 MB DDR, 8MB Flash
Number of I/O card interface	1	2
Number of PMC interface	1 : PCI(33MHz/66MHz, 32bit/64bit)	0
Clock frequency of user FPGA	50 MHz	50 MHz
Network interface	gigabit Ethernet port	0
OS (CPU on FPGA)	Timesys Linux (PowerPC 440)	--

A Block diagram of data flow in the new advanced base board



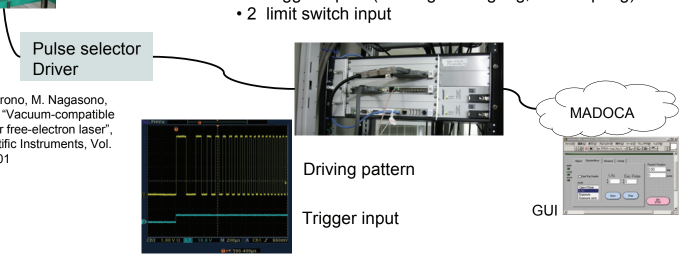
4. Applications

We applied our board as a controller of a pulse selector for free electron laser*** .



Controller of pulse selector
= Flexible logic-reconfigurable VME board
(**Basic base board** + **DIO mezzanine card**)

- Trapezoidal driving pattern in TTL output (～88000pps)
- 3 trigger inputs (arm trig. driving trig, and stop trig)
- 2 limit switch input



***T. Kudo, T. Hirono, M. Nagasono, and M. Yabashi, "Vacuum-compatible pulse selector for free-electron laser", Review of Scientific Instruments, Vol. 80, (2009) 093301

5. Conclusions

- We created a development environment for the flexible logic-reconfigurable VME board.
  →The development environment shortens the period of firmware development.
  → We could applied to various control system, including the pulse selector controller, in the short time.
- We developed the new base board.
  → The new base board supports fast data transfer.

➡ **The capability of the flexible and logic-reconfigurable VME board was increased.**

Author's E-mail : hirono@spring8.or.jp