A Pulse-Pattern Generator Using LabVIEW FPGA

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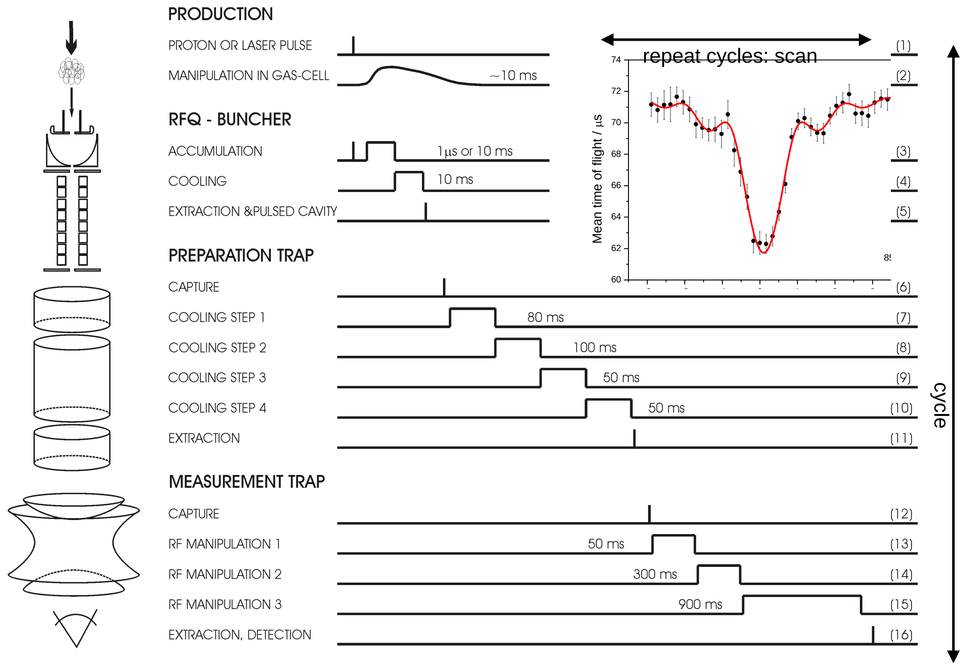
Motivation

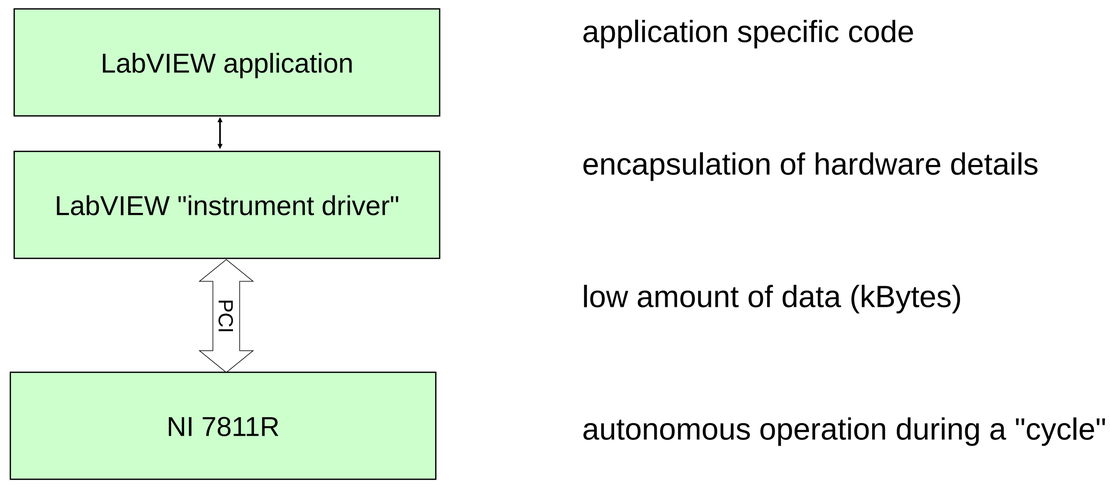
Timing system for small (~10 m) ion trap facilities



- synchronization to external trigger conditions
- synchronize/adjust steps with 10ns precision
- pattern width 64 bit, each bit is one output line
- pattern is applied for a specified time
  - 10000000 @ t = 0 µs
  - 10000001 @ t = 1.2 µs
  - 11000101 @ t = 235246.875 µs
  - ....
- more requirements: loops, *fast context switching* ...

Implementation

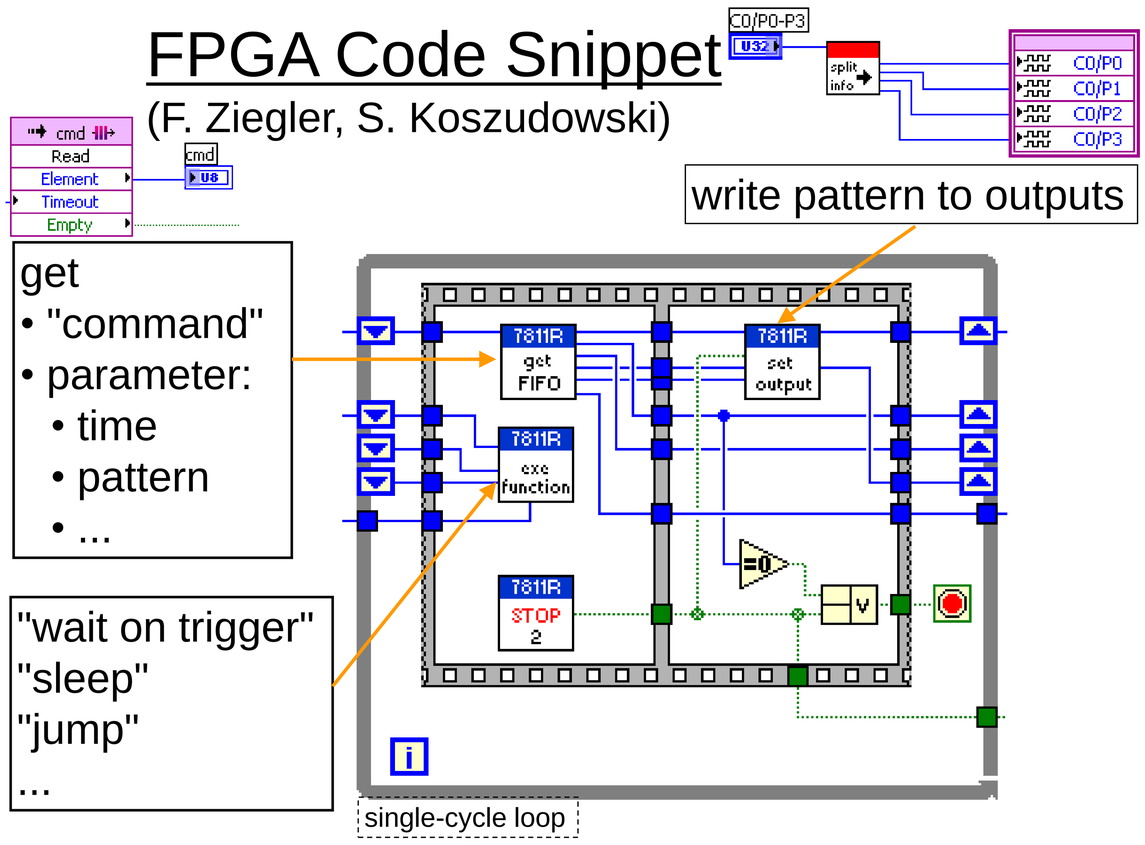
- PCI/PXI-7811R board from National Instruments (≈ 1500,- €)
- 160 digital lines (TTL)
- Virtex II, 1 M gates
- 80 MHz single-cycle loop (12.5ns resolution)
- timing of bit patterns independent of
  - operating system
  - data-bus
  - PC, CPU, ...
- can be programmed by FPGA non-experts using LabVIEW
- then: VHDL code generation, Xilinx tool chain, ...



Procedure: Commands with user defined pattern data are uploaded to onboard memory. Pattern

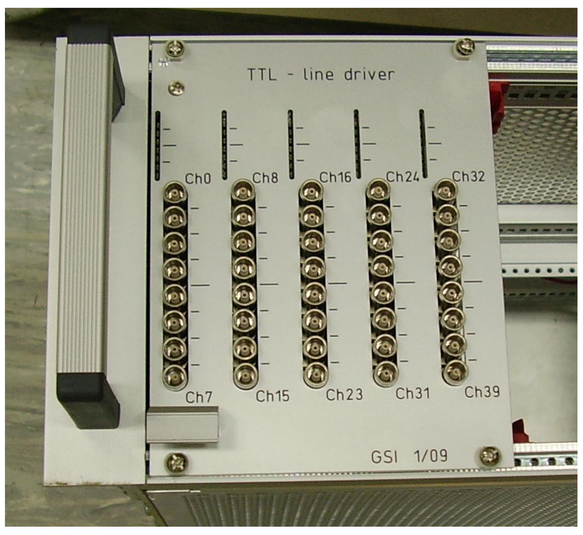
FPGA Code Snippet

(F. Ziegler, S. Koszudowski)



Status and Remarks

- presently (2009) used at six experiments*
- FPGA compile time about 50 minutes (PIV, 3GHz)
- code also runs on other FPGA cards 7813, 7831, 7833, PCI/PXI
  - –requires re-compilation of FPGA code
  - –requires modification of LabVIEW code (just a typedef, but ...)
- PCI: no synchronization to external reference clock
- PXI: phase-locked to 10 MHz PXI clock
- NI boards provide TTL output @ 4 mA on high density plugs
  - –some devices need more current at trigger inputs
  - –users connect one TTL output to multiple trigger inputs
  - –users want Lemo plugs!
  - –solution: signal conditioning using a TTL line-driver module (see picture)



*References

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