THE FIRST STEPS OF THE BEAM INTENSITY MEASUREMENT OF THE SPIRAL2 INJECTOR

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Abstract

The Spiral2 Injector [3] includes several diagnostics. The first ones implemented are Faraday cups, Emittancemeters and DCCTs. Two types of acquisition for the beam intensity measurement on the Faraday cup are being developed. They are based on different industrial electronic boards. The goal of the first type of acquisition is to determine an average intensity value using a traditional acquisition VME board (32 multiplexed channels). This was carried out for the beam tests on the low beam energy line at LPSC Grenoble in May 2009. The second type of acquisition is to perform a measurement synchronized with the beam pulse, the purpose of which is to provide the peak value. Due to the bandwidth of the expected signals, it is necessary to be able to sample at 1 Msamples/second with ADCs of which the resolution is greater or equal to 14 bits. We chose the couple of ADAS ICV108 (4 Megabytes buffer, event and flip/flop modes) and ICV178 (8 analogue inputs with high accuracy) COTS VME boards. The associated EPICS software is in progress and will also be integrated into the Emittancemeters acquisition.

AVERAGE INTENSITY MEASUREMENT

Context

The command control to measure the average intensity with 2 Faraday cups [1] was tested at LPSC Grenoble in June 2009 for the first beam tests with the q/a=1/3 ion source.

Hardware

The electronic board to perform the current to voltage conversion (I/V) was designed by Ganil/GEM Lab [2]. This conversion is on 2 ranges to allow the measurement of low and high currents. These 2 ranges are simultaneously available and filtered. The bandwidth is about 0.5 Hz.

Our standard VME platform with ADAS [4] boards is used. To measure this average intensity the ADAS ICV150 with 16 bits resolution and 30 Ksamples/s is used. Two channels are permanently scanned for each cup.

The Ganil/GEM board also provides two levels of reference current, one for the low level of 150µA and another for the high level of 5 mA. These reference currents are sent to the Faraday cup itself. These tests are carried out through the binary input/output ADAS ICV196 board.

The Emerson Motorola MVME5500 is the CPU chosen for all the VMEs of the project.

Software

EPICS has been chosen for Spiral2 accelerator control command [3]. The operator has to choose the range. EDM displays the channel corresponding to the selected range. The reference current tests permit the measurement chain from the Faraday cup itself to electronics, cables, EPICS database and EDM display to be validated.

An offset measurement procedure is available. It is done with beam cut off and then the current intensity is displayed with or without offset.

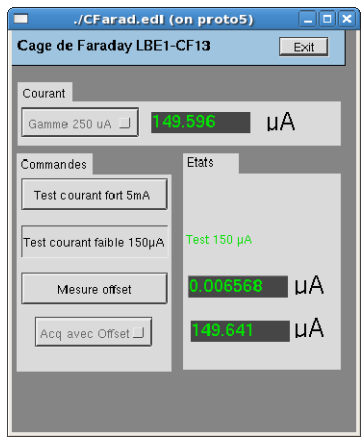

Figure 1: Display to manage different procedures.

SYNCHRONISED INTENSITY MEASUREMENT

The Purpose

The beam intensity of the Injector of Spiral2 will be measured in 2 ways:

- beam destructive measurement with four Faraday cups in the Low Energy Beamline Transfer
- non-destructive measurements : 2 DCCTs in the Low and Middle Energy Beamline Transfers.

The horizontal and vertical transverse emittances will be measured by Emittancemeters (scanner type).

The diagnostics have to be used during commissioning, the daily process and the machine studies.

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During the tuning phases, to limit the beam average power intercepted by the diagnostics, the duty cycle will be increased progressively until commuting to CW mode.

The general principle for this synchronized acquisition is to start the acquisition at the pulse start, to buffer the digitalised data, to calculate the peak or the average value for each pulse or several pulses and to display the pulse shape.

The foreseen signals bandwidth for the ion source and deuteron source is about 50 KHz. Consequently, our constraints were to choose a board with a sampling at 1 M samples/second, an external trigger to synchronise the acquisition with the beam pulse and ADCs 14 bits resolution.

Like VMEbus was the chosen standard for Spiral2 command control, another constraint was to choose a COTS VME board.

The Solution

These major specifications lead us to select these boards:

- an ICV178 16 bits resolution, 8 analog inputs and 1.2 Msamples/s
- a controller board ICV108

Both boards communicate via the VME I/O lines P2. The ICV108 includes an external trigger, a RAM buffer of 4 Mbytes and runs in "Single Event" or "Flip/Flop" modes. The block transfer rate could reach 76 Mbytes/s in VME64.

CLOSE COLLABORATION WITH ADAS

The NEXEYA/ADAS Company provides these boards with no drivers. The ICV108 and ICV178 boards offer numerous possible configurations. Therefore, ADAS has helped us in the understanding of these boards and in the development of our VxWorks software to test the processes.

These boards are not yet used in the accelerator domain but their perrenity is not a concern. The couple ICV108/ICV178 is used for real time calculations of the harmonic distorsion for generators on the Airbus A380 and soon on the Airbus A400M.

HOW WE USE THE ADAS ICV108 BOARD

4 Mbytes RAM Dedicated to Measurements

In the ICV108 board a space memory of 4 megabytes in A32 space is used as a temporary buffer. This space is built of 2 equal size RAMs of 2 Megabytes each one. Following the acquisition mode, this space is seen as only one RAM (single event mode) or as 2 RAMs (Flip/Flop mode).

The board also uses a space memory of 256 bytes (short I/O) for the configuration of registers.

Patterns Table of the ICV108 Board

The ICV108 comprises a pattern table 32K x 16 bits in A24 space. This table contains the basic pattern used to save the data in the RAM. The same pattern is repeated in the RAM throughout the acquisition. The pattern can be divided into subpatterns. For our first applications, we divide the pattern into 10 identical subpatterns, each one composed of 4 channels. The header of each pattern includes a timestamp. The timestamp clock is the sampling frequency. The timestamp is taken between the gate activation and the start of the numeric conversion. Consequently, the components of a pattern are first the timestamp and then ten times four channels.

There is also the possibility to tag in the header the pattern number.

Data and timestamps are transferred by P2 VMEbus.

```
0x83800000:  0000 0007 a945 7ff3 8049 7ff7 a945 7ff3
0x83800010:  804b 7ffb a97f 7ff5 804b 7ff3 a945 7ff3
0x83800020:  804b 7ff9 a945 7ff5 8047 7ff5 a943 7ff1
0x83800030:  804d 7ff7 a943 7ff7 804d 7ff9 a941 7ff1
0x83800040:  8047 7ff9 a943 7ff7 804b 7ff5 a943 7ff1
0x83800050:  804b 7ff9 0000 00a7 a945 7ff3 8049 7ff5
0x83800060:  a947 7ff3 8049 7ffb a941 7ff3 8049 7ff7
0x83800070:  a941 7ff3 804b 7ff7 a947 7ff3 804d 7ff7
0x83800080:  a941 7ff5 8049 7ff5 a947 7ff5 8049 7ff7
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Figure 2: Data in ICV108 RAM.

SOFTWARE

Processes

For all Spiral2 VME applications, EPICS with the real time system VxWorks is used [3].

Analogue input and waveform EPICS devices are developed. They are composed of several tasks. At the VME startup, ICV108 and ICV178 board initialisations are launched, followed by tasks in charge of acquisition, DMA transfer and calculations.

At each beam pulse start, the acquisition is automatically triggered. The data acquired by the ICV178 ADCs are transferred by P2 VMEbus in the ICV108 RAM following the defined pattern. At the end of the last pattern, the ICV108 generates an interrupt on VMEbus. When the program detects this interrupt, it carries out the DMA transfer via Tundra Universe II chip embedded in the Emerson Motorola MVME5500 CPU. The time spent in this transfer is not yet optimised. The synchronisation between this DMA transfer and the interrupt detection is managed by a binary semaphore.

Some measurements have been taken. At 1 Msamples/s, for a beam pulse width of 20 milliseconds, the transfer between the stop of acquisition into the CPU, takes 440µs, including interrupt.

Management of the Sampling Frequency

Concerning sampling frequencies, these boards have a lot of possibilities. For our applications, on ICV178 board ADCs, we do an oversampling by 16 and consequently the acquisition sampling frequency can be selected by software between 250 Ksamples/s and 1 Msamples/s. At present, the choice of sampling frequency is the responsibility of the user and is not automatically managed following the beam pulse width.

For the intensity measurement of the Emittancemeters Faraday cups, the sampling frequency will remain at 250 Ksamples/s and only the Flip/Flop acquisition mode will be used.

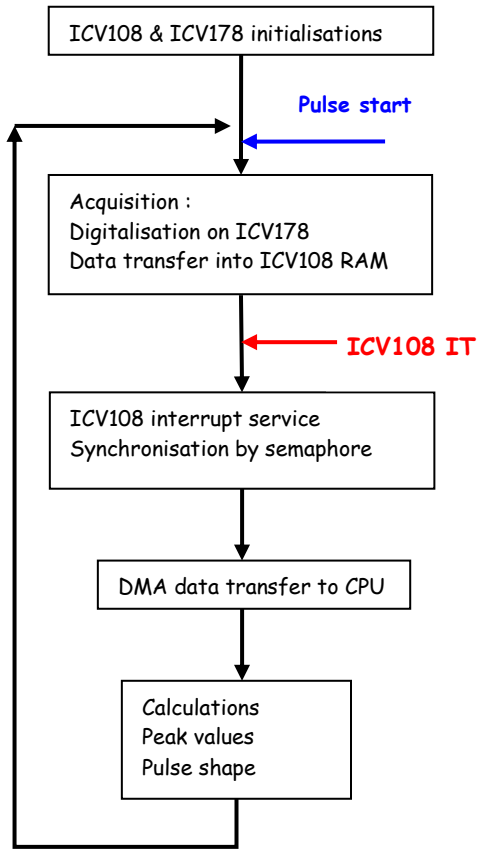

Figure 3: EPICS software.

Status

At present, EPICS Analogue input record for peak value, waveform record and Analog output record to control sampling frequency are available. The user requirements are very wide and the difficulty is to find common configurations. Beam tests will take place at the end of the year.

MVME5500 CPUS

During our first weeks of tests, 3 CPUs crashed only due to software bugs. One of these bugs was a memory-write outside the allocated memory, both flash banks were corrupted.

This problem of flash corruption consecutive to a software bug is known from Wind River Support. It concerns MVME5500 CPUs flashes (Intel Strata types). Therefore, protection of flash banks is required.

In the MVME5500 VxWorks board support package, the protection bit for flash memories is not set to be able to use flashes as disk through TFFS module. Our lab has modified VxWorks kernel to protect flashes. This measure seems effective.

Due to the necessary memory to work with ADAS ICV108 board, the address space VME A32 has been extended to all the space system memory available.

INTERFACE TO THE PLC INTERLOCK

Diagnostic interlocks and controls are achieved by a Siemens S7-300 PLC with its own supervisory system. PLC also includes a free Modbus/TCP server to establish the communication with an EPICS Input Output Controller. Only modbus functions 3 and 16, read and write array of 16-bits words, are implemented in the server, so inputs/outputs are carried out through gensub and waveform records in EPICS databases to share data with the PLC.

ACKNOWLEDGEMENTS

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