TIMING SYSTEM UPDATE FOR SNS*

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Abstract

A timing system is a crucial subsystem of every accelerator, responsible for orchestrating the entire machine cycle by cycle. The current SNS (Spallation Neutron Source) timing system is based on the modified BNL (Brookhaven National Laboratory) solution which in turn is based on previous systems at other sites. The timing master is a collection of low functionality VME building blocks that are highly dependent on creative software to achieve the needed system functionality. The implementation technology of the whole system is backdated, making it impossible to build and maintain spares and boards for machine upgrades. At SNS we chose a roadmap which would allow a gradual upgrade of the timing system without having to redesign everything at once and yet provide a path for future modernization of the infrastructure. This paper presents progress on the timing master and receiver card, which will provide us with more flexible control and greater reliability by tremendously reducing the component count while still retaining compatibility with existing timing receiver units. The designs emphasize the use of FPGA (Field Programmable Gate Array) technology in a way that simplifies the supporting software. The design of the system is a collaborative effort of ORNL and Cosylab.

SNS TIMING

Project Goals

The goals of the timing upgrade project align with the long term goals of the SNS. The facility is now in a multiyear program to increase the power delivered to the target and increase the beam availability to 95%. In addition, planning is underway for a power upgrade and a second target station.

The SNS project is the outcome of collaboration between several of the national labs. Responsibility for building the timing system went to Brookhaven due to the experience BNL has with accelerating ions. The SNS timing system is based on the RHIC (Relativistic Heavy Ion Collider) timing system and shares much of the same hardware modified only to match the slightly different event link frequency requirements of the SNS [1]. Development work for the SNS timing system started in 2001 and now many of the components used in the system are obsolete.

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What we have now is an inability to buy or produce spares or boards for the planned construction, and aging equipment in an era of decreasing down time targets. It was time to start planning a way to start an upgrade.

MAKE / BUY DECISION

Early in the process of planning a timing system upgrade, the MRF (Micro Research Finland) system was evaluated [2]. In fact, a minimal MRF system was installed and used in the laser wire diagnostic system to take advantage of the MRF's ability to synchronize with the RF clock. The MRF is able to generate scheduled events and send real time data. Due to the MRF system's inability to be frequency agile, the variable frequency ring clock could not be transmitted over the MRF system. Using the MRF system would mean a redesign of the three systems in the accelerator which include the LEBT/MEBT (Low Energy Beam Transport/Medium Energy Beam Transport) chopper controller, the ring RF systems, and the extraction kicker timing hardware. The balance of the timing hardware would also have to be replaced with MRF hardware. The cost of the hardware, the cost of the software effort, time, and risk required to change are simply prohibitive.

MASTER

Goals for the New Timing Master

The first design criterion was to replicate the existing system signals and timing. Secondly, it was to eliminate several weaknesses and points of failure in the existing hardware and software design of both the master and existing receivers. Thirdly, reduce downtime by allowing for software reboots and upgrades while keeping the accelerator on-line for an immediate return to operation. Finally, we eliminate the need to add hardware in most

Table 1: Essential Timing Master Requirements

Name	Value
Event Link (EL)	NRZI Encoding at 32 times the ring clock. Events are 8 bits with start bit, parity, and stop bit.
Real Time Data Link (RTDL)	NRZI Encoding, data words include an 8 bit frame number, 24 bits of data, and an 8 bit frame CRC.
Software	EPICS IOC on top of real time application.
External IO	Machine Protection System status, beam on target data, MPS Status, beam on target data

cases to expand the timing master, making it possible to meet new timing requirements. Designing a flexible system in addition to owning the design gives us the ability to adapt to all challenges in the future.

Key Timing Master Design Features

In the sections that follow, we will describe the key features of the master design.

Table 2: Comparison Between Old and New Timing Master

Feature	Old	New
Generation of fixed events	Gate cards triggering an event encoder. Events constantly have to be re-timed. Not expandable without adding hardware.	Table driven with a memory location corresponding to a position in the event link time line.
Event collision control	Protects cycle start but not the extract event. MPS events jostle fixed events.	Fixed events are selected first. No jostling of events is allowed.
Super Cycle Pattern (Run time)	Generation of non 60 Hz events requires participation by software	Implemented entirely in hardware. Will be described below.
RTDL Generator	Spans multiple cards, needs pre-loaded map table, not expandable without adding hardware	Single memory mapped array that includes per frame enable bits.
Generation of RTDL Data	All done in software including message CRC.	Hardware maintains time stamp and other critical RTDL data even when the software is not running.
System Hardware Requirements	1 CPU board, 1 Event encoder using 3 boards, 4 timing delay gates, 1 RTDL encoder using 5 boards, a GPS board, a frequency counter, a fan out module, a utility module, and a set of bus extenders for two VME crates.	1 CPU Board, 1 timing master board, and one GPS board.

Clocking

The event link clock is provided by an external arbitrary waveform generator that is locked to a GPS (Global Positioning System) receiver. The signal generator provides a nominal 33.84 MHz +- 6% sine wave to the front panel of the master board. This frequency is 32 times the ring frequency. A hardware clock adds the ability to hold the clock frequency even if the master clock fails.

Event Generation

There are three ways an event can be generated in the new timing system. At highest priority is the "fixed" event, defined to occur at a specific delay from cycle start. Next in priority is the "hardware" event. A hardware event is encoded after a trigger is received from an internal or external source. The lowest priority event is the "soft" event, which is written into a FIFO by the IOC (Input Output Controller) software and encoded if no fixed or hardware events are available.

The event pattern for a cycle is held in VME accessible memory as one byte per location corresponding to one event per turn. The SNS timing system generates several fixed events including cycle start, RF events at seven different rates, source on, beam events, six diagnostic events at three different rates, and extraction events.

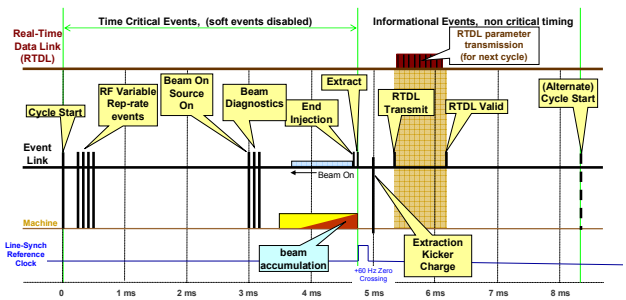

Figure 1: SNS beam timeline within a cycle.

The VME mapped event table allows events to be moved on the timeline and new fixed events to be easily implemented.

Table 3: Example Event Table Entries

Location	Event Number	Event Name
0	1	Cycle Start
20	52	RF 60
21	53	RF 30
4000 (variable)	36	Beam On
4010(variable)	37	Diagnostic Fast
4020(variable)	38	Diagnostic Slow
5048	40	End Inject
5050	39	Extract
5150	48	Extraction kicker charge

Pattern Generation (Super Cycle)

The timing system has to provide timing for all phases of machine operation from system testing during maintenance outages all the way up to full power. Tune up involves operating the beam at rates as slow as 0.1 Hz while other systems are operated at fractions of 60 Hz during start-up. This led to the design of a 10-second or 600-cycle super cycle and algorithms to compute smooth patterns [3]. Even when machine systems are operating at different rates, source at 10 Hz, RF at 20 Hz, and kickers at 30 Hz the timing system must find a way to place beam pulses into time slots when everything is pulsing at the same time. This is accomplished with the pre-computed super cycle pattern.

Table 4: Example Pattern Table

Beam On	60 Hz	30 Hz	20 Hz	10 Hz
1	1	1	1	1
0	1	0	0	0
0	1	1	0	0
1	1	0	1	0
0	1	1	0	0
0	1	0	0	0
0	1	1	1	1

Table 5: Example Configuration Table Rows

Event	20 Hz	30 Hz	10 Hz
RF-20	1	0	0
RF-30	0	1	0
RF-10	0	0	0
Ekick	0	1	0
Srce	1	0	0

In this example the source is at 20 Hz and the extraction kickers are set to run at 30 Hz

The pattern table is 600 words with a word for each cycle of the repeating 10-second pattern. Each bit in the word represents a different repetition rate from 1 to 60 Hz plus a bit for the beam repetition rate calculated by software.

A third table merges the cycle table with the super cycle table to produce the event stream on the event link. The event table has a location for each possible event number that is sent by the timing master. When an event arrives from the event multiplexer, the event's configuration is looked up and used to decide if an event should be transmitted on the current cycle. The decision criterion includes the pattern bits from the super cycle table as well as bits from external hardware and software controlled registers.

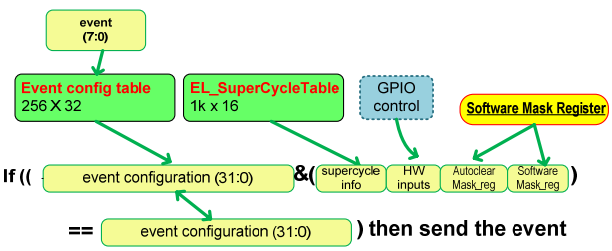

Figure 2: Operation of the event link pattern filter.

TIMING RECEIVER

The new timing receiver is in the process of being designed at the time of this report. It will combine the functions of two of the BNL cards and provide IOC access to the full RTDL (Real Time Data Link), hardware event triggers, software event triggers, and event and RTDL diagnostic functions. The FPGA selection will be one of the new Xilinx chips providing good availability into the future. We plan to build a few of these cards now to relieve the spares crunch caused by newly evolving requirements for timing ports and then build a larger production run for the second target station and power upgrade later.

Receiver Features

The receiver will use existing FPGA code from previous projects, including the chopper controller and timing master. An ADN 2816 clock and data recovery chip will receive the event link [4]. A similar chip is being used in the front end chopper controller and has rock solid performance there. The receiver board will include test points and components to support automated testing.

CONCLUSIONS

The SNS is working toward a 95% beam availability goal during scheduled operation. Historically, timing master outages have been mostly software related. This is no different than any other IOC. By keeping the machine running without software help, timing master outages can be limited to minutes, not hours. Should a hardware replacement be needed, a single board has the advantage over a complex multi-board system. This project will implement a timing master that can be restarted without disrupting the machine and will make available master and receiver spares built with up to date components.

REFERENCES

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