DEVELOPMENT OF A NEW PHASE DETECTOR FOR THE APS LINAC*

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Abstract

An effort is being made to upgrade the Advanced Photon Source linac rf phase detector system. The decision was made to replace the current phase measurement system, which is based on a Los Alamos National Laboratory designed analog vector detector module, with a digital I/Q method. As an initial step we reconfigured one of our current 8-channel, 14-bit ADC designs, originally developed for the storage ring beam position monitor system, to perform the I/Q sampling and the phase and magnitude computations. This paper discusses the current board design, proposed modifications to optimize the board for this application, and the field programmable gate array design.

INTRODUCTION

The Advanced Photon Source (APS) linac radio frequency (rf) system utilizes phase detectors to assure that properly phased rf is applied to the linac accelerating structure. The phase detector design currently in use on the APS linac is based on an analog vector detector module originally designed by Los Alamos National Laboratory (LANL). The LANL design is still usable, but we are struggling to maintain adequate spares. We therefore are developing a replacement system based on digital I/Q methods. As a prototype, we chose a circuit board originally designed as part of the APS storage ring beam position monitor (BPM) system [1]. It is based on the Altera! [2] Stratix II field programmable gate array (FPGA) and eight high-speed analog-to-digital converters (ADCs) manufactured by Analog Devices [3].

BACKGROUND

The BPM data acquisition board, shown in Fig. 1, consists of eight Analog Devices AD6645, 105MSPS ADCs, an Altera! Stratix II FPGA and a Arcturus Networks [4] uC5282 microprocessor module, which acts as the input/output controller (IOC) processor. The flexibility of the FPGA allowed us to easily modify the design to create a phase measurement board, employing I/Q sampling techniques. The board also has 12 digital TTL outputs, several trigger inputs (SMA and SMB) for synchronization, a reference clock input and two fiber signals that are currently configured to interface event signals from the APS event system.

Prototype Board Shortcomings

This design is a good starting point for our prototype; however, because this board was so tightly coupled to the unique needs of the BPM system, there are a few obstacles to overcome. Of primary concern were the interface connectors on the front panel along with the signal levels of the external trigger inputs.

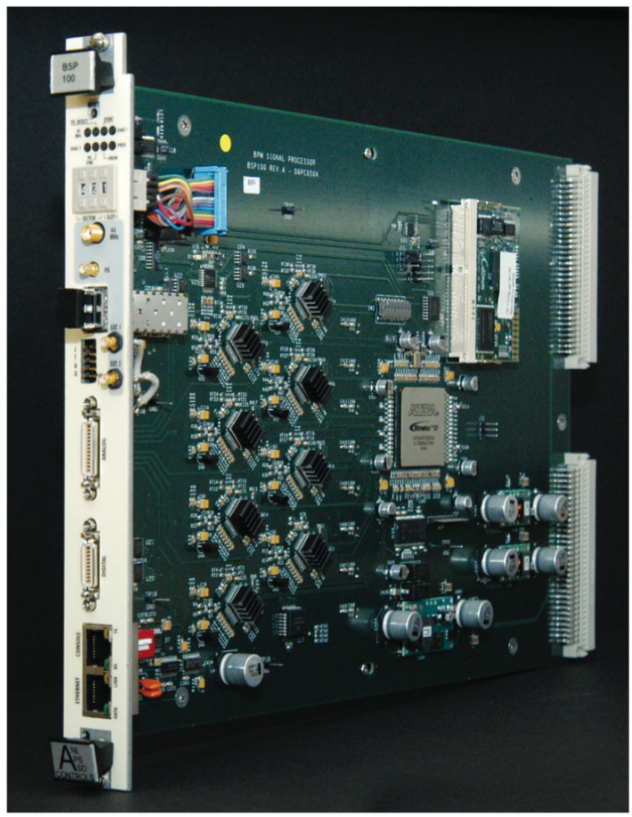

Figure 1: BSP100.

The analog inputs to the board are received differentially via a 26-pin 3M™ MDR-style [5] connector. This was done because all the analog signals of the BPM system originate in a single chassis and it was desirable for integration and maintenance to have a single analog connector to remove, rather than eight. While this was convenient for BPM system integration, it is a hindrance to our phase detector design because the sources of our signals are not concentrated.

Another issue to overcome is that the external reference input expects LVTTL logic levels. The external reference that we will use for the phase detector is an rf level.

Prototype Adaptations

The first obstacle we had to overcome was how to apply the analog signals to the board. The prototype board requires differential analog signals on a 26-pin MDR-style connector. Fortunately, a 2U height breakout panel was available for board testing of the BPM system. Each of the eight analog signals breaks out to an isolated BNC connector. The eight signals are routed on a PC board to

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maintain impedance matching, then to a MDR connector, which connects to the front panel via the standard MDR cable used in the BPM system.

The second obstacle to overcome was the fact that the external reference input expects a LVTTL signal. We want to use a reference signal for our phase measurement that is a ±1V, 20-MHz CW rf signal. Again, we were fortunate to already have a module designed that converts rf to LVTTL.

While these adaptations allowed us to initiate our prototype test, they also will degrade our measurements.

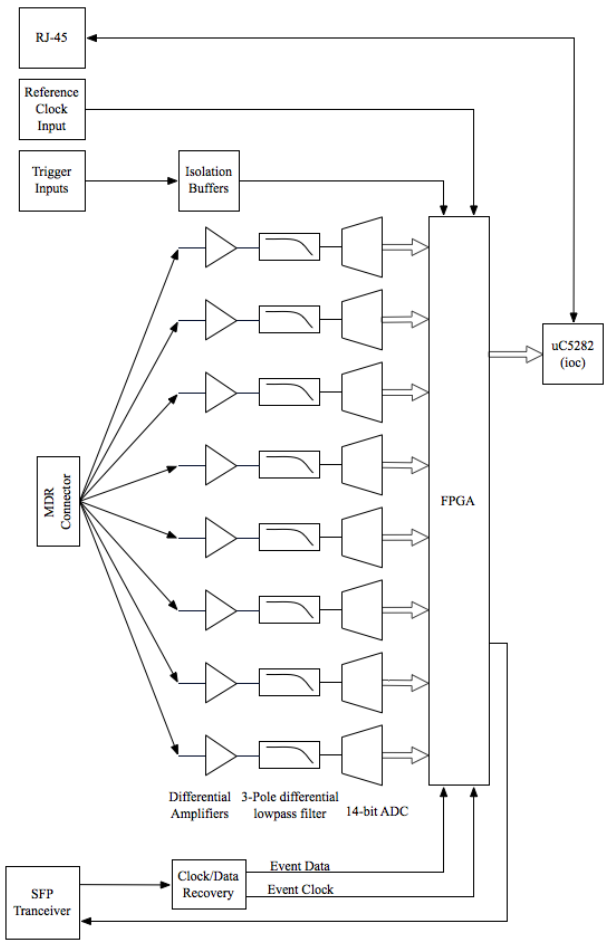

Figure 2: Simplified prototype block diagram.

PHASE DETECTOR DESIGN

Figure 2 shows the overall phase detector prototype block diagram. In addition to what is shown in the block diagram, the prototype setup included a rf-to-LVTTL 6U board (APS model RFC100) and a 6U board to convert the APS event signals from 820-nm ST fiber connector to 1300-nm small-form pluggable LC fiber connector (APS model FCF100).

The prototype analog front-end uses differential amplifiers because the BPM requires the signal bandwidth to extend down to DC. The phase detector does not require the DC component of the signal; therefore, this portion of the circuit will be modified to provide transformer coupling.

FPGA Design

The heart of the phase detector design is the FPGA. The FPGA, shown in Fig. 3, accepts a 20-MHz reference signal that is synchronous to the down-converted linac rf. It multiplies the reference by 4x, to 80 MHz, via a phase locked loop (PLL). This signal is used to control the ADC sampling, the I/Q sampling, and the phase/magnitude calculations. The FPGA accepts an external trigger signal that is synchronous to the linac beam repetition rate as well as APS event data. Both the external trigger and the event data are synchronized with the 80-MHz signal from the PLL and may be used to control the data acquisition. Either one or the other of the synchronized triggers can be selected to trigger phase measurements and the waveform recorders.

Internal to the FPGA, the phase detector design is divided into two banks, each with its own reference signal. The reference signals will be applied to channel 0 and channel 4. These reference signals are subtracted from the three associated inputs to improve measurement accuracy.

Waveform recorder memory is provided at each step of the process to record intermediate results. This memory is accessible by the control system for display and troubleshooting. Circuitry is included so that the user can select a region of interest and the number of samples for the average calculation. The region of interest is typically the so-called “sweet spot” of the pulsed signal.

FUTURE PLANS

Given the drawbacks previously stated, we plan to redesign the circuit board to optimize it for our purposes. Among the changes we plan to make are replacing the MDR connector with individual SMA connectors. The MDR connector was appropriate for the BPM system because all the analog signals were concentrated in another chassis. For this application, the rf signals will be originating at several locations in the linac rf system and transported over Heliax® [6] cables.

Since the rf signals will now be single ended, we will change to transformer coupling to maintain ground isolation. A feature of transformer coupling is that the secondary is naturally differential and high impedance, allowing it to be directly interfaced to the differential input of the ADC. This reduces the active component count by eliminating the differential amplifier.

The 20-MHz reference signal input will be changed to accommodate the rf nature of this signal. A high-speed, low-jitter component will be used to convert the 20-MHz reference signal to a LVPECL differential signal for transmission to the FPGA.

The boxcar average circuit will be replaced with a true 14-tap, low-pass, finite impulse response (FIR) filter. Data taken previously with a similar setup demonstrated

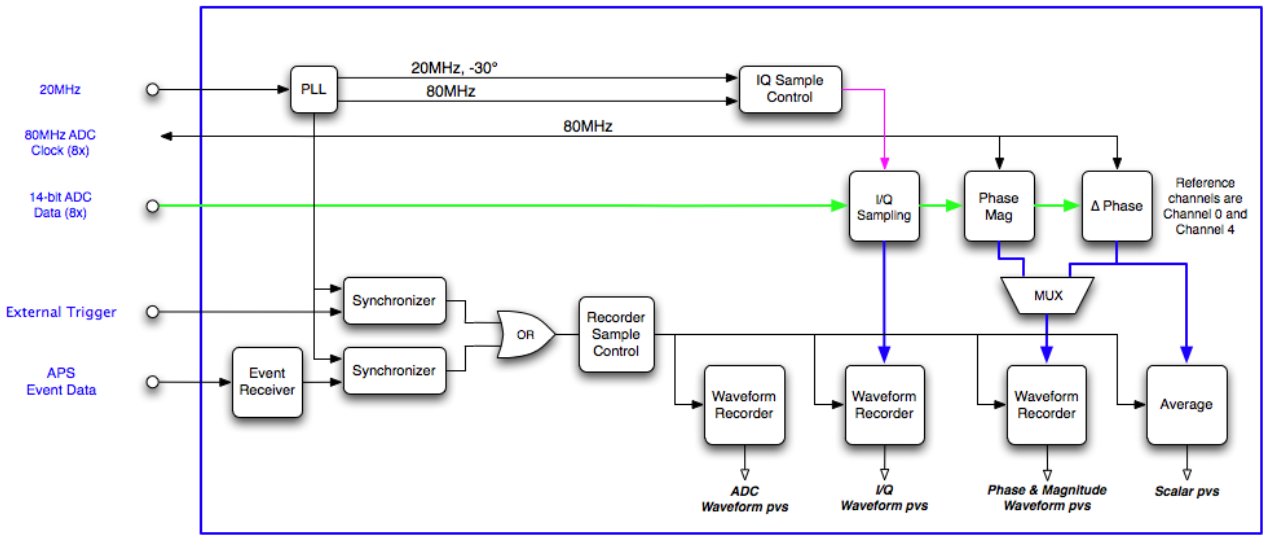

Figure 3: FPGA block diagram.

that the 14-tap FIR filter improves the signal-to-noise ratio of the measurements.

Additional discussions are under way to consider changing the original design idea from strictly a phase detector to a fully functional low-level rf board with digital-to-analog converters. This would be an easy transformation to accomplish. There is plenty of room on the C-size, 6U-height circuit board to add the additional components. There is also sufficient room in the FPGA to accommodate the additional firmware.

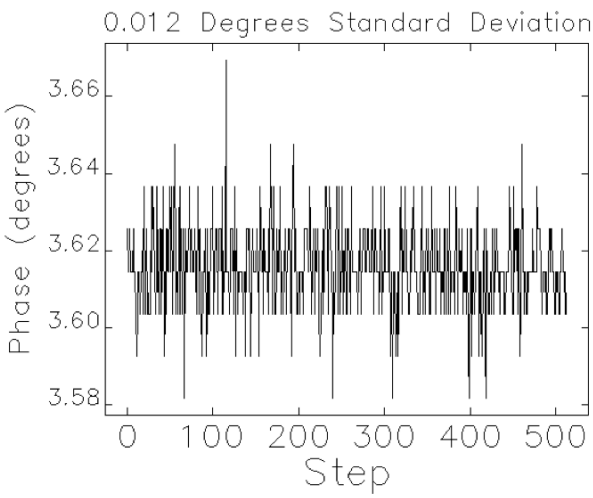

Figure 4: Noise floor measurement without averaging.

SUMMARY

The Advanced Photon Source is in the process of upgrading the linac rf phase detector system. The decision was made to replace the current phase measurement system, which is based on a Los Alamos National Laboratory designed analog vector detector module, with a digital I/Q method. As an initial step we reconfigured one of our current 8-channel, 14-bit ADC designs, originally developed for the storage ring beam position monitor system, to perform the I/Q sampling and the phase and magnitude computations. This paper discussed the current board design, proposed modifications to optimize the board for this application, and the field programmable gate array design.

Preliminary evaluation demonstrates a system noise floor of 0.012° rms. Figure 4 shows 512 samples of the phase measurement minus the reference signal but without averaging.

ACKNOWLEDGEMENTS

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We would also like to thank David Jefferson for his help setting up the rf test stand to test this design.

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