DESIGN OF AN XFEL BEAMLINE DAQ SYSTEM

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Abstract

We have designed the control and the data acquisition (DAQ) system for the SPring-8 XFEL beamlines. The XFEL generates ultra-short pulsed coherent X-ray laser with the 60Hz beam repetition rate. The DAQ system has to synchronize with the accelerator beam operation cycle to obtain correlations between incident X-ray and experimental data. Two-dimensional x-ray detector that is under development will output data at every beam shot, and the total amount of data reach to petabyte. The key technologies to make a success of the DAQ system are a tagging system that identifies X-ray shot of the 60Hz X-ray pulse, and a real-time compression system that helps fast massive data handling. In this paper we will describe preliminary design of XFEL beamline DAQ system and will discuss future plan.

INTRODUCTION

In 2006, the XFEL project was designated as one of the key technologies of national importance in Japan and launched as a five-year construction project at SPring-8. XFEL generates high brilliant and coherent laser at a 0.1nm region. The maximum brightness of XFEL reaches one billion times that of SPring-8. By using the X-ray laser many researches of the novel region such as single molecular analysis of protein become possible.

To realize these advanced experiments, high performance two-dimensional X-ray detector and the real-time DAQ system are most important. We have started manufacture of a CCD detector with a multi-readout ports design (MPCCD), 2kx2k 50-micrometer square pixels, and 5 M electrons of a full-well capacity at each pixel. Most of XFEL experiments require shot-by-shot identification of X-ray laser pulse and that must be synchronized control with the accelerator operation. The detector should record whole frame data at an XFEL repetition rate of 60Hz. In XFEL, close cooperation of the control system and the DAQ system becomes especially important. A control framework, MADOCA [1], is used for overall of XFEL controls. The MADOCA was originally developed for SPring-8 and we will apply the MADOCA to the DAQ system to control detector, trigger system and related matters.

BASIC DESIGN

The specifications required to the DAQ system is shown in table 1. Total bandwidth comes from MPCCD, which has 2048 x 2048 pixels, reaches 3.52 Gbps and data amount for every 24 hours exceeds 38 TByte. A brute force DAQ system cannot record such a huge amount of data without any loss. The front-end system is designed by using the camera link interface that excels in abilities of real-time triggering and high-speed data transfer. By dividing the detector into eight segments of 1024 x 512 pixels the bandwidth for each segment is decreased to 440Mbps that is supported by a basic configuration of the camera link.

Table 1: Performance Requirements for the DAQ System

Number of pixel	4 M Pixel
Depth	14 bit
Repetition Rate	60 Hz
Total bit rate	3.52 Gbps
Bit rate par segment (8segs)	440 Mbps
Data amount (24h)	38.05 TByte

The divided segment is operated with synchronized trigger system. It is necessary to mark tag on the data to recognize the simultaneity of the collected data. It becomes possible to distinguish an antecedent of the observational data by containing information of the time of each shot of the accelerator operation. In the past, we have developed a tagging system for the user experiment of the SCSS test accelerator. This tagging system, made as IP core on FPGA of the flexible and logic-reconfigurable VME board [2], has the I/O interface of the parallel and the serial to deliver tag information to user's experimental equipment. We will construct the DAQ front-end system in addition to the data compression function on this tagging system and integrate it into MADOCA control system. The MPCCD requires highly I/O performance to the latter parts of the DAQ system such as network and storage. An in-line data compression system is a key technology to achieve the consummate DAQ system easily. The data compression reduces the cost for the storage system greatly by suppressing total amount of data. It is necessary to take account to loss-less compression and indispensable as a data compression technology.

Because of a lot of computer power is required for the analysis of the XFEL experiment, we plan a real-time data analysis using the next-generation supercomputer under construction by RIKEN. Figure 1 shows the conceptual design of the data acquisition and analysis system. This system is composed by four elemental technologies enumerated as follows.

1) DAQ front-end that collects data from detector, compresses data with loss-less, and transfers compressed data to storage system

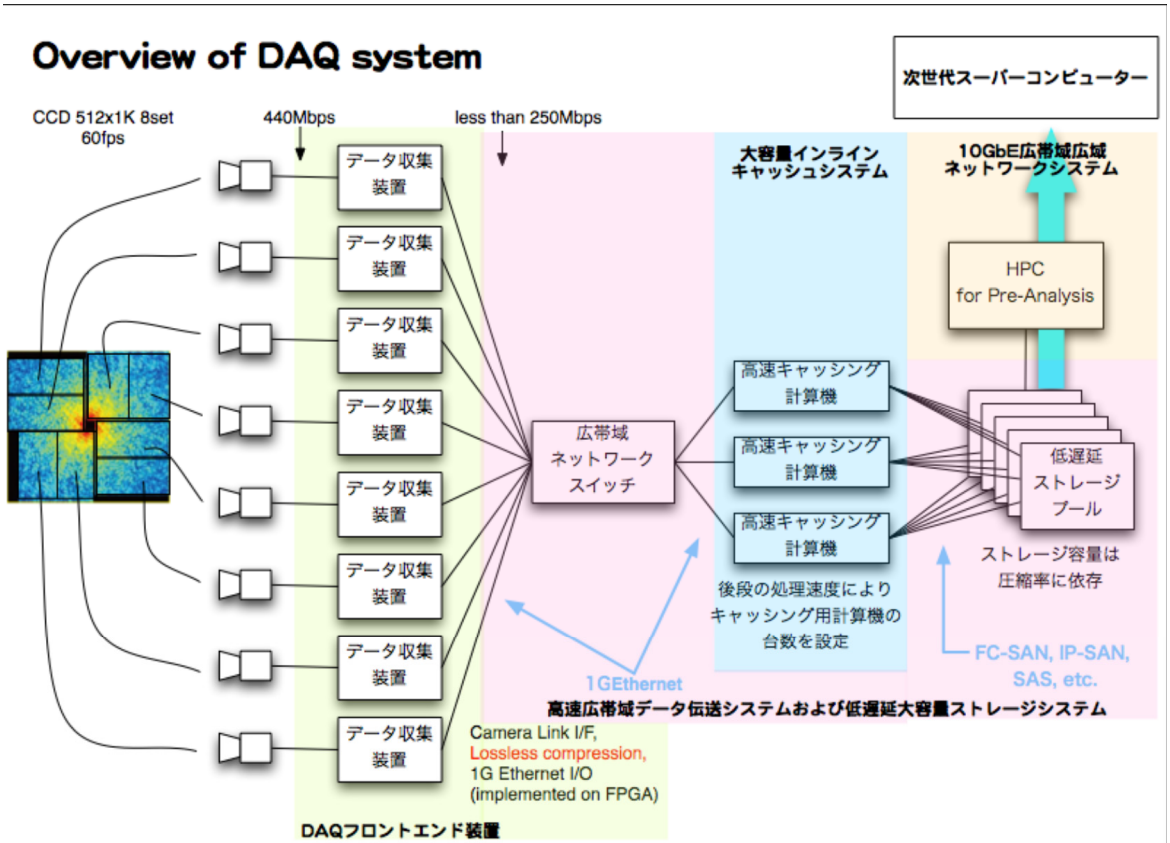

Figure 1: Overview of DAQ system. There are four elemental technologies of DAQ front-end, high-speed network and low-latency storage, in-line cache and wideband WAN.

2) High-speed wide-bandwidth data transmission system and the large capacity low latency storage system
3) Large capacity in-line caching system for data loss protection and event building
4) Wide-bandwidth wide area network to achieve real-time data analysis that uses next-generation supercomputer

In this paper we will describe about the DAQ front-end system. And also we will discuss a preliminary designed of a storage system and an in-line caching system. As a WAN, one 10Gbit Ethernet will be introduced for XFEL at April of 2011 by using SINET4. However, research and development of the data transfer application on the WAN are future tasks.

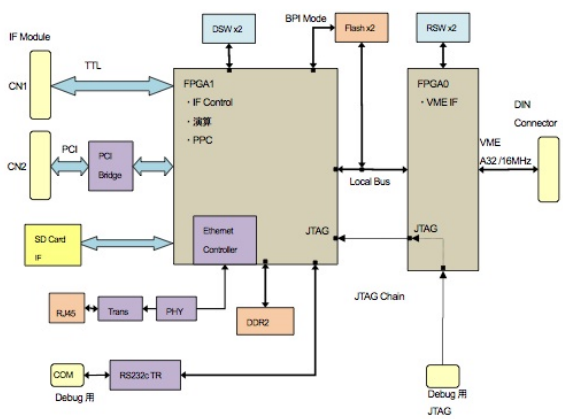

Figure 2: Block diagram of DAQ front-end system.

DAQ FRONT-END SYSTEM

DAQ front-end system is designed based on the flexible and logic-reconfigurable board that has VME form factor. The system transfers data from the MPCCD to a storage system and carries out a loss-less compression with in-line data stream. It contains one camera link interface, two Gigabit Ethernet interfaces and FPGA processing units for real-time compression. Block diagram of the DAQ front-end system is shown in figure 2. Camera link interface card is connected with the baseboard by 2500Mbps bandwidth LVTTL bus. One of Gigabit Ethernet interfaces is built on 64bit/66MHz PMC slot. The other that is connected via local bus is included on the baseboard. One is the interface for the recording of whole data, and the other is used for a real-time monitor of sampling data. It is necessary to obtain less than 2Hz at intervals of the data sampling.

An algorithm of in-line compression will be implemented as FPGA logic. And also we implement functions of the camera link I/F control, the tagging system, and the trigger control etc. on FPGA. Virtex-5 FXT (XC5VFX70T) that has 1 PowerPC 440 processor block is selected. Linux is running on the PowerPC for making the data transfer applications. Figure 3 shows the block diagram of the function implemented on the FPGA.

The FPGA driven by a trigger signal synchronized to operation of the XFEL accelerator. The trigger signal is passed to trigger interface Intellectual Property (IP) core that generates tag information. An image data of the MPCCD that is sent soon after the trigger signal is captured by camera link interface IP core. And the IP core of camera link transfers data byte-by-byte to compression IP core consecutively. A compressed data is transferred to DRAM, which is accessible by Linux. And then processing task is passed to Linux from IP cores which process in pipeline. A data path that skips compression IP core to monitor raw image data for diagnostics is also prepared. IP cores are connected via local bus and are developed by using embedded development kit (EDK).

As a compression algorithm we adopted range coder that is an entropy coder similar to the arithmetic coder, because it is fast and simple algorithm suitable for FPGA. Furthermore, it has no license problem and calculating procedures. Compressibility is about 50% at the test image. Implementations of Linux and board support package (BSP) for PCIbus controller are already finished.

Packing of several frame data will be able to suppress the I/O overhead at the data transfer of gigabit Ethernet. We are studying most appropriate network transfer method in the DAQ system. It is important that the construction of both the network system with 3~4 Gbps bandwidth and the petabyte-class storage system in the initial operation phase of the XFEL project.

FUTURE PLANS

A first test system of the DAQ front-end will be assembled by early 2010.

At a point of risk management, we studied several implementations for the DAQ front-end system concurrently. For instance, to enhance a real-time performance of the data transfer we consider a option of reflective memory that is low latency shared network instead of Gigabit Ethernet. Or to obtain more compressibility we will be able to implement JPEG 2000 or other compression algorithm.

It is necessary to design the network and the storage system immediately. We are studying several storage systems and filesystems paying attention to the latency and the throughput performance.

REFERENCES

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[2] T. Hirono et. al., “Development of Flexible and Logic-reconfigurable VME Board”, Proc of ICALEPCS 2007, Knoxville, USA, (2007)