POWER SUPPLY CONTROL SYSTEM OF NSLS-II

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Abstract

The NSLS-II is a third generation light source and has many unique requirements for its power supply system. The NSLS-II power supply control system is designed to meet these requirements. The control system is designed as a general system to control different power supplies in the storage ring and the injection systems. The power supply control system is used for the slow and fast orbit feedback systems of NSLS-II. This paper describes the architecture of NSLS-II power supply control system.

INTRODUCTION

As a third generation light source, NSLS-II is designed to achieve many stringent requirements for beam parameters, such as low emittance, high beam current and stable beam orbit [1]. To obtain a precise and stable beam control, NSLS-II power supplies and their control system is required to have high precision, high stability, high reliability and fast response [2][3].

On the other hand, the NSLS-II power supply control system should be a generic low cost design so that the large number of power supplies share the same control architecture. The control system should support different accelerator subsystems such as storage ring, injection system, slow and fast orbit feedback system. NSLS-II power supply and control groups are working together to finish the architecture design. We are making good progress in the detailed design. This paper first presents the overall architecture and then gives the detailed discussion of the subsystems.

NSLS-II POWER SUPPLY CONTROL SYSTEM ARCHITECTURE

Figure 1 shows the architecture of NSLS-II power supply control system in one cell. A cell is a section of the NSLS-II storage ring. There are a total of 30 cells in the storage ring. The control system consists of five subsystems: regulator module, power supply interface (PSI), power supply control (PSC), cell controller, and EPICS IOC.

NSLS-II power supply is using an analog approach for current regulation. The control data which includes an analog setpoint value and digital commands flows from the EPICS IOC to the cell controller through a Gigabit Ethernet link. The data link from the cell controller to all PSCs (in the cell) is a redundant 100Mbps Ethernet link. The BNL-designed protocol called synchronous device interface (SDI) is running on the link. From the PSC to the PSI, the data is transmitted through a 50Mbps fiber optic link. On the PSI, the setpoint data is used to set the DAC output. The DAC analog output is wired to the regulator module to set and control the power amplifier (or power converter) to get the correct magnet current. The digital portion of the data (command) is used to control the power supply states such as on, off or standby.

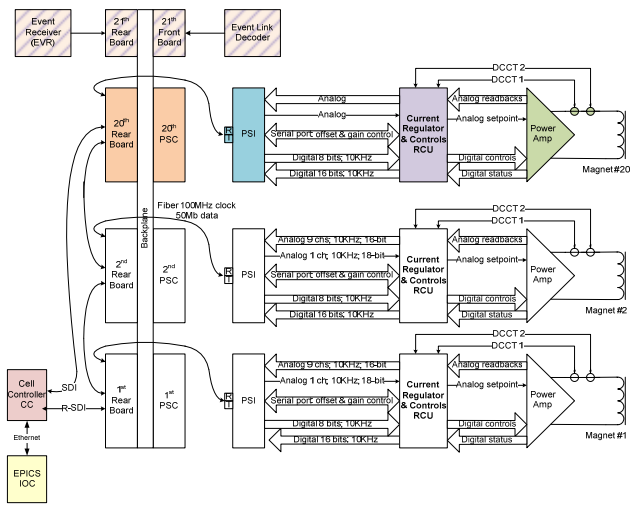

Figure 1: NSLS-II power supply system.

In the other direction, the monitor data (includes analog readback values and digital status) moves from the regulator to the PSI, then to the PSC, the cell controller and the EPICS IOC.

Unlike other accelerator control systems, power supply control doesn't have a "standard" architecture. Different accelerators use different approaches [4][5][6][7]. The NSLS-II power supply control system incorporates Ethernet and fiber link as the communication media. Ethernet is used because it is a long-lasting, well supported and low cost technology. The fiber link is used to cut the ground loop between the power supply and its control system.

NSLS-II POWER SUPPLY CONTROL SUBSYSTEMS

The NSLS-II power supply control system consists of five subsystems. The functions for each subsystem are clearly defined. The subsystems work together to provide a complete control data flow from the control room to the power supplies.

Regulator Module

The current regulator module is a standalone 1U chassis. The main function of a current regulator is to provide a feedback loop for magnet current.

The current regulator module receives two signals: the analog setpoint from the PSI and the magnet current measured from a DC current transformer (DCCT). The

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current regulator compares these two signals to get an error signal. The error signal is amplified and goes through proportional-integral-derivative (PID) loop to drive the power amplifier. The PID loop can be tuned to get a precise magnet current and reasonable response time. The gain and offset of the regulator module can be remotely adjusted through the power supply control system.

The current regulator module also receives other diagnostics analog signals (such as power amplifier voltage and ground current). It buffers these signals to the PSI where ADCs convert them into digital signals.

A PIC microcontroller is used to convert the digital commands from PSI to power amplifier specific commands. The microcontroller also converts the power supply specific status and sends it back to the PSI.

Power Supply Interface (PSI)

Figure 2 shows the block diagram of a PSI. The form factor is a 1U standalone chassis. The main function of PSI is to provide a stable analog voltage. To get good long term stability with a cost effective solution, we incorporated a self-calibrating 18-bit DAC chip (AD760) on the PSI. Most of its error is from the temperature drift, which is about 10ppm/^{o}C. To get the best stability from this DAC, a temperature controlled daughter board is designed. The daughter board uses a temperature feedback to provide 0.1^{o}C temperature stability. The DAC chip is assembled on the temperature controlled daughter board. Therefore, the DAC stability is well controlled.

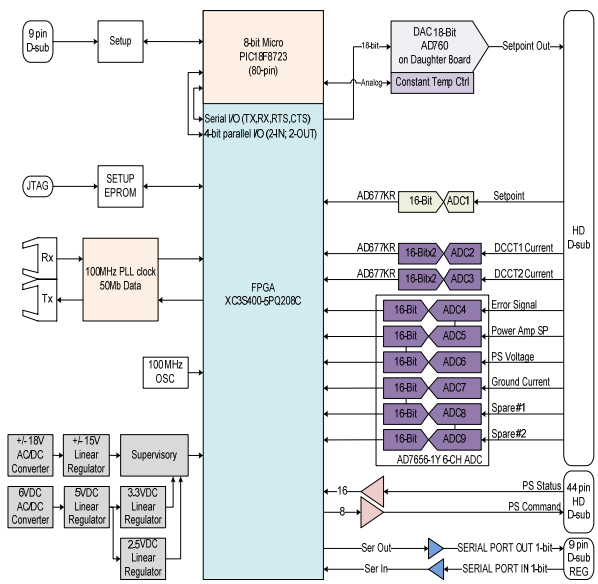

Figure 2: Power supply interface.

The PSI also digitizes the diagnostics analog signals. It can digitize up to 10 analog signals at a 100 KHz sample rate. All the ADC chips have 16-bit resolution.

The PSI communicates with the PSC through a 50Mbps fiber optic link. The PSC sends the setpoint and command to the PSI. The PSI responds to the PSC with readback values and status.

Power Supply Controller (PSC)

The PSC has two major functions. The first function is to provide communication between a PSI and a cell controller. The communication protocol is called synchronous device interface (SDI). Power supply SDI link is running through Ethernet. It has dual redundant ring structures to ensure the communication reliability and fault tolerance. The SDI link minimizes the cabling connections (each PSC just needs to connect with its neighbor PSCs). The second major function of PSC is to provide a large memory for storing large amount (half Gigabyte) of data. The data can be used for power supply ramping waveforms or various diagnostic data.

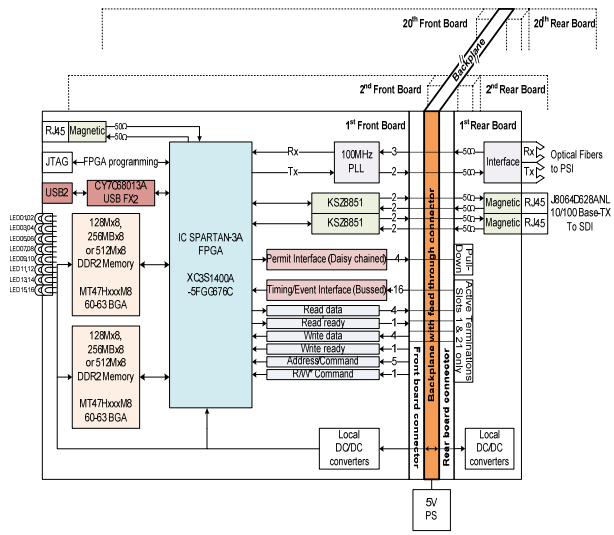

Figure 3: Power supply controller.

Figure 3 shows the block diagram for a PSC. Up to 20 PSCs are installed in a 3U Euro chassis. Each PSC module consists of a front board and a rear board. The rear board host communication connectors such as the fiber connector, and the SDI Ethernet connectors. Most of the logic chips (such as FPGA, memory, Ethernet MAC/PHY etc) are located on the front board. The front board also has a Ethernet port. This port is running UDP/IP protocol. It can be used for local diagnostics or remote control by a control system.

The backplane of the PSC chassis provides power to each PSC. There is a trimming buffer module in the last slot (slot 21). The module is used to receive timing triggers from NSLS-II timing system (EVR). The timing triggers are distributed to all PSC cards through the backplane.

Cell Controller

The cell controller links NSLS-II beam position monitor (BPM) system and power supply control system. It is the critical system for beam orbit feedback. There is one cell controller in each cell. The cell controller interfaces with local BPM units to collect the BPM data. The cell controller uses fiber optic link running SDI protocol to distribute BPM data to the whole storage ring

through a deterministic and reliable communication method [8] called fiber optic synchronous device interface (SDI). The SDI link transmits all the BPM data to each cell controller. Each cell controller uses the data to conduct reverse matrix calculation and get new corrector power supply setpoints. The setpoints are sent to power supply control system through power supply SDI link, which use 100Mbps Ethernet as the communication link.

The cell controller uses a Gigabit Ethernet as the interface with the control system. Standard TCP/UDP/IP protocol is used to transfer data to the control system.

EPICS IOC

NSLS-II control system uses a standard VME crate to host EPICS IOC. To improve the reliability, the VME crate is built with dual redundant, hot-swappable power supplies. Also many control/monitor features are built into the crate. These features include temperature monitor, voltage monitor, fan speed monitor and control.

The EPICS IOC is running on a MVME3100 processor board. RTEMS is chosen as the real time operating system. For the power supply control system, EPICS drivers for cell controller and for PSC will be developed by NSLS-II control group.

NSLS-II POWER SUPPLY CONTROL SYSTEM PROGRESS

The prototype units of the regulator module and PSI module have been built and tested. The standalone regulator module tests show <5 ppm medium term stability. Figure 4 shows the picture of the PSI prototype.

We are in the progress of testing an integrated system that consists of a PSI, a regulator module, a power amplifier and a magnet. We are measuring all the performance parameters of this power supply system. These measurements will give us a better understanding of the performance of NSLS-II power supply control system.

The PSC and the cell controller are in the design stage. The EPICS IOC running on MVME3100 has been well tested.

Figure 4: Prototype of PSI.

CONCLUSIONS

NSLS-II power supply control system is designed not only to meet the stringent requirement for NSLS-II beam control, but also to provide a reliable, generic architecture for various power supply controls. We are making good progress in the subsystem design.

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