FPGA MEZZANINE CARDS FOR CERN's ACCELERATOR CONTROL SYSTEM

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Abstract

Field Programmable Gate Arrays (FPGAs) have become a key player in modern real time control systems. They offer determinism, simple design, high performance and versatility. A typical hardware architecture consists of an FPGA interfaced with a control bus and a variable number of digital IOs, ADCs and DACs depending on the application. Until recently the low-cost hardware paradigm has been using mezzanines containing a front end interface plus custom logic (typically an FPGA) and a local bus that interfaces the mezzanine to a carrier. As FPGAs grow in size and shrink in price, hardware reuse, testability and bus access speed could be improved if the user logic is moved to the carrier. The new FPGA Mezzanine Card (FMC) Vita 57 standard is a good example of this new paradigm. In this paper we present a standard kit of FPGA carriers and IO mezzanines for accelerator control. Carriers form factors will be VME, PCI and PCIe. The carriers will feature White Rabbit support for accurate synchronization of distributed systems. Initial plans include IO mezzanines for 100Ms/s ADCs and DACs, digital drivers and inputs, high accuracy time tag units and fine delay generators.

INTRODUCTION

CERN's Controls (BE-CO) group supports a standard kit of hardware modules which are used by equipment groups in the design and development of control system solutions. These equipment groups include Beam Instrumentation (BI), Radio Frequency (RF), Beam Transfer (BT) and Electrical Power Converters (EPC). The support includes access to hardware documentation, user manuals, Linux device drivers, C/C++ libraries with usage examples and test programs.

The standard modules kit is meant to satisfy the most common controls hardware needs and includes support for analog I/O at different sampling speeds and precisions, digital I/O with interrupt support, synchronization and various fieldbusses. Traditionally, the cards have covered these needs in the VME form factor. Due to price/performance considerations, the controls group decided to support industrial PCs in addition, generating a need for hardware modules in PCI and PCIe form factors. In order to satisfy this request in the most efficient way, we decided to adopt a carrier/mezzanine approach, which results in several benefits:

- One mezzanine can be used in VME, PCI and PCIe carriers.
- Reaction times to new user requests are reduced. Most new needs concern types with an FPGA and and I/O interface not yet supported. With a carrier/mezzanine split, the complicated part of the problem – placing and routing a complex FPGA PCB – is avoided, and only a simple mezzanine design is needed.
- Different equipment groups have different specialties and work can be split in a more rational way. For instance, the CO group can supply the carriers, the BI group can design an ADC mezzanine and the RF group can contribute a DDS mezzanine to the kit.

The selected mezzanine format must not impose a shared non-deterministic bus between the carrier and the mezzanine, as was the case with the PCI Mezzanine Card (PMC) standard, and must allow high-speed digital signaling at its interface to support the latest electrical standards and applications. In the past, the RF and BI groups at CERN came up with their own custom solutions to the problem because there was no standard fulfilling their needs. With the advent of the VITA 57 FMC standard, there is now a generic and versatile solution to the problem of modular FPGA-based hardware design.

THE FMC STANDARD

The FMC standard [1] was approved by the American National Standards Institute (ANSI) in July 2008 and specifies two types of Ball Grid Array (BGA) connectors to mount a mezzanine on a carrier. The Low Pin Count (LPC) connector provides 160 pins capable of multi-Gb/s transmission speeds. The High Pin Count connector (HPC) extends the pin count to 400. Modules can be single or double width. The outline of a single width module can be seen in Figure 1.

The size of the mezzanines – roughly a 6 cm side square for the single width card – is deliberately small in order to guarantee that carrier designers can provide an area below the mezzanine without any hot integrated circuits. For example, FPGAs with dense designs clocked at several hundreds of MHz could represent a severe cooling problem if placed directly below the mezzanine. The FMC sizes are therefore smaller than some existing standard and non-standard solutions, but one has to bear in mind that the philosophy in the FMC standard is to place the absolute minimum possible in the mezzanine – signal conditioning and possibly conversion – and to delegate all digital complexities to the FPGA design in the carrier.

Pins are agnostic in the sense that their function, sense

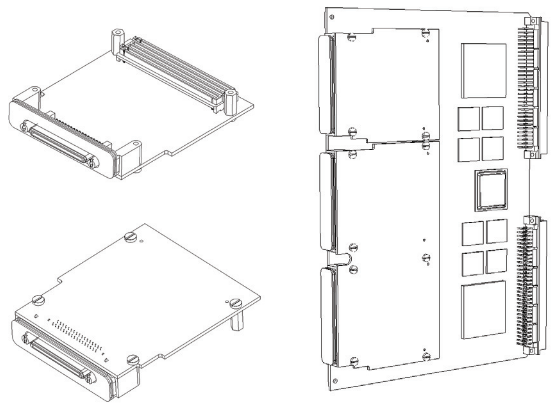

Figure 1: Single width FMC outline, and carrier with single and double width FMCs, courtesy of VITA [1].

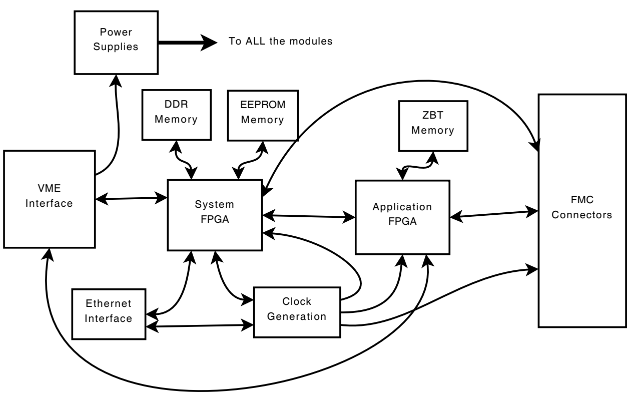

Figure 2: Block diagram of CERN's VME FMC carrier.

– input or output – and electrical standards are defined at FPGA configuration time. The mezzanine must implement an EEPROM which can be read from the carrier's FPGA through an I2C link after power-up. With this information, the FPGA can be configured with an appropriate bit-stream to support the specific type of plugged-in mezzanine.

USE CASES

Carriers developed at CERN will feature White Rabbit (WR) [2] support. This means that the carrier will be able to send precise phase-compensated clocks and triggers to the mezzanines all around CERN's accelerator complex. The WR data link achieves this using clock recovery circuits and precise phase measurements and shifting. Figure 2 shows the block diagram of the CERN VME carrier, and some use cases for the FMC-WR combination can be seen in figure 3. The first and trivial application is to make a timing receiver card using the WR features of the carrier and a simple LVTTL I/O FMC. The second one uses WR's low latency and determinism to connect sensor and actuator FMCs together in a large distributed feedback system. Global Orbit Feedback would be a good example of

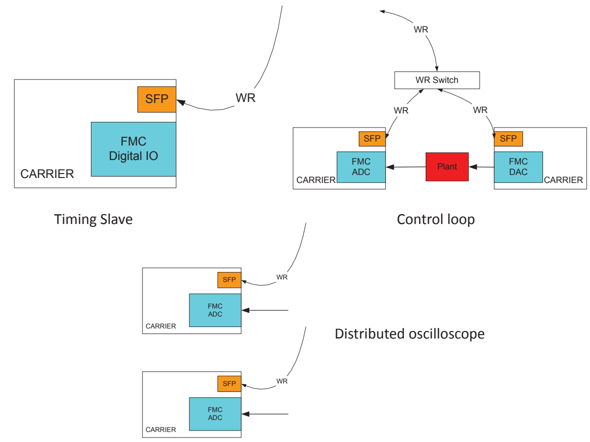

Figure 3: Different use cases for interconnected FMC carriers at CERN.

this kind of systems. The third one enables a completely synchronized distributed oscillospe application. Trigger pulses can be provided by users anywhere and they are time-tagged very precisely by a Time to Digital Converter (TDC) FMC. This FMC will provide ns-level Coordinated Universal Time (UTC) time tags thanks to WR's ability to compensate for transmission delay in its distribution of UTC. Once the trigger is detected, the carrier hosting the TDC FMC can send a WR broadcast or multicast asking some of the ADC FMCs to freeze their circular acquisition buffers. These buffers will be the result of sampling using WR-derived clocks, so each sample will have an associated UTC time tag which the software can use to select the data to be sent to the higher layers in the control system in order to generate a time-coherent display of the signals in the control room. Current solutions to this problem involve sending trigger pulses to all oscilloscopes, with the associated cabling costs and lack of scalability for large accelerators.

OPEN HARDWARE CONSIDERATIONS

One important characteristic of the FMC projects at CERN is that they are being carried out under the Open Hardware (OH) design paradigm. OH adoption and rationale are heavily influenced by its counterpart in the software world and imply a series of technical and managerial decisions:

- All design files – including schematics and PCB layout – must be published in order to benefit from peer review and enable easy remote collaboration. This feature has already been experienced with great success during the design of the WR switch.
- All files needed for producing the hardware – including gerber, Bill Of Materials (BOM) and manufacturing files – must also be published in order to enable potential users and companies to build and try out hardware in the easiest possible way.

- Peer review is a good thing, but an additional effort must be made in order to design hardware which is as re-usable as possible. In terms of reducing duplication of effort, the hardware community is certainly lagging behind the software one. This problem is already visible inside large scientific facilities, not to speak about inter-lab collaboration. Think about the number of developers currently designing a 100 Ms/s ADC in all labs, independently and making the same – or different – mistakes. The choice of the FMC standard combined with OH is a potential – if partial – solution to this problem.

In order to provide a web-based platform on which hardware designers around the world could collaborate, CERN's BE-CO Hardware and Timing section teamed up with Cosylab to produce the Open Hardware Repository (OHR) [3]. The OHR is made up of a combination of four open software tools:

- A twiki space is created for each project, allowing easy editing by all project members and sharing of information such as plannings, meeting minutes and design specifications.
- Each project automatically creates a mailing list including all team members. For this we use the mailman list manager.
- A subversion repository for all design files – including drivers, firmware, gateware, schematics and PCB files – is provided for each project. Versioning and easy web access for all design partners is thus seamlessly integrated in the collaborative tool.
- Finally, bugs and new user requests are handled using bugzilla.

The role of companies in the OH paradigm is by no means reduced. They can participate during the design stage, and of course get paid for it. They can also manufacture and test the cards and sell them with an associated support. This would give the end user the best of the custom and Commercial Off The Shelf (COTS) worlds. On one hand, hardware teams in labs could give good local support to their users because they would have all design information. Pricing abuse temptations would also cease to exist. On the other hand, the burden of managing component stocks, ensuring good yields in production and the time-consuming testing process would be delegated to companies. From the point of view of companies, there are also advantages in this scheme. For example, a company could get introduced to a highly specialized design area – such as fine timing – with the help of many knowledgeable designers in the labs. Also, as a given piece of open hardware becomes more and more popular, the customer base gets bigger and bigger.

One important issue to consider when adopting OH is that of Intellectual Property (IP) rights in particular and licensing in general. The GNU Public License (GPL) does not match well the needs of the OH community because it is based on copyright, and copyright protects the expression of an idea, not the idea itself [4]. This means that GPL would be very easy to bypass in the case of a circuit schematic. Among the ongoing efforts to come up with a suitable license for OH, the most advanced is currently the Open Hardware License (OHL) [5]. The OHL is more a contract than a license and is built around the idea that whoever takes your design and uses it should agree to not sue you for patent infringement concerning that design. The viral effect of OHL is similar to that of GPL, and this might represent a problem for some companies, so work is ongoing to design a new license that would not have such a strong viral component, in the philosophy of the Lesser GPL (LGPL) for software.

CONCLUSION AND OUTLOOK

CERN's BE-CO Hardware and Timing team has decided to embrace the FMC standard in order to give the best possible internal hardware support for control systems while keeping design effort reasonable. The carrier/mezzanine approach allows to cover many form factors with minimal duplication of work. In addition, all carrier will support the new White Rabbit synchronization system, opening the way to new applications in the field of distributed real-time systems.

All FMC and WR developments are being carried out under the Open Hardware paradigm, which implies a major rethink of the role of companies for hardware design, procurement and support. One important aspect to cover in this field is that of Intellectual Property Rights and licensing. Work is underway to find a suitable legal framework for this new paradigm.

In the near future, we will start looking for commercial partners to produce, test, sell and support its new generation of controls systems hardware. Before the end of 2009, the VME and PCIe carriers should be finished, as well as FMCs with 100 Ms/s ADCs and 10 Ms/s DACs.

REFERENCES

[1] VITA 57 FMC standard
See `http://www.vita.com/fmc.html`.

[2] J. Serrano et al., "The White Rabbit Project", these Proceedings.

[3] See `http://www.ohwr.org`.

[4] John R. Ackermann, *Towards Open Source Hardware*, 34 U. Dayton L. Rev. 183 (2009)

[5] See `http://www.tapr.org/ohl.html`.