

THE CONTROL SYSTEM OF THE ATLAS PIXEL DETECTOR*

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Abstract

The innermost part of the ATLAS experiment is a pixel detector, built of 1744 individual detector modules. To operate the modules, readout electronics and other detector components a complex power supply and control system is necessary. While the hardware is mainly built by units which are specially adapted to the needs of the pixel detector, the control software has to support these special needs, while in parallel it is embedded into the ATLAS wide control system. Core of the pixel detector control is a PVSS based SCADA system in combination with a finite state machine. An overview on the pixel detector hardware and a report on the commissioning of the final control system will be given. We concentrate on the description of the finite state machine and its interaction with several additional protection routines.

INTRODUCTION

To achieve an optimal performance of the DCS (Detector Control System) its segmentation follows the mechanical construction, the modularity of the services, and the readout units.

The pixel detector is a segmented silicon-based semiconductor detector. The barrel part consists of three cylindrical shells which are equipped with staves to install the detector modules. In both end caps three identical disks carry the detector modules.

Each module has 16 front end chips which connect the pixel sensors with the readout electronics and which are supervised by the Module Control Chip. A detector module is the smallest unit on which the control system can act on.

Via optical fibres the data are transmitted to the data acquisition system. While the on-detector part of the optical link is located on small special PCBs, the optoboards, the off-detector part is built by the BOC (Back of Crate) cards, which are installed on the back side of the VME readout crates. As six or seven modules of a half-stave, respectively disk sector, are read out via one optoboard, these 272 readout groups form the second important DCS unit.

In order to remove the high power dissipated by the front end electronics, a C₃F₈ based evaporative cooling system is installed. Each two disk sectors, respectively two staves share one cooling circuit. These 80 cooling circuits determine the third segmentation which must be taken into account when the DCS groups are defined.

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HARDWARE

The hardware was chosen and built according to the special needs of the pixel detector. The sensitive front end chips, which are produced in deep sub micron technology, can be destroyed even by short over-voltages. Sensors and electronics must be protected against overheat, and a high granularity of the services is desired for an optimal tuning. As a large part of the equipment will not be accessible over long periods, a very high level of reliability is necessary.

Detector modules, optoboards, the environment and the readout crates are the objects which must be monitored, supplied and controlled, see Fig. 1. The DCS hardware can be grouped into three groups: the monitoring units, various power supplies, and the interlock system.

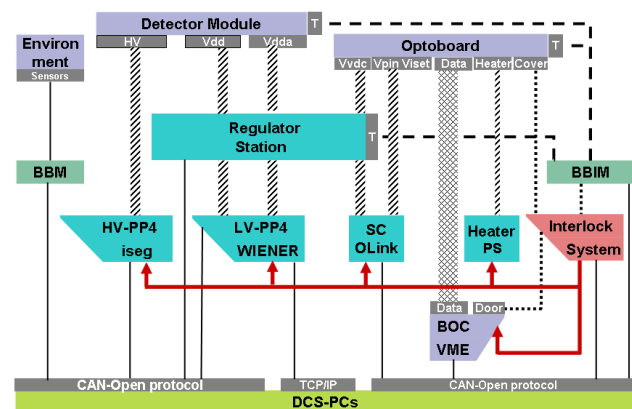


Figure 1: Overview of the DCS hardware.

Besides the HV and LV power supplies, all components of the pixel control system are custom made. Their core is the ELMB (Embedded Local Monitor Board), the ATLAS wide used front end control unit with a 64 channel ADC and a CAN (Controller Area Network) interface [1].

The monitoring units, BBM and BBIM (Building Block Monitoring, respectively Interlock and Monitoring) are responsible for the readout of the humidity and temperature sensors. The power supply system consists of the commercial LV and HV supplies (provided by W.IE.NE.R, Burscheid, Germany and iseg, Rossendorf, Germany), the custom made regulator stations, the SC-OLink (Supply and Control of the OptoLink), and multichannel current measurement units, LV-PP4. For the Heater PS also units from W.IE.NE.R are used.

Especially the detector modules can be irreparably damaged due to heat ups. To protect all sensitive equipment against overheat, and human beings against risks due to the infrared lasers of the optical link, a complex interlock system is installed.

The different units are connected via CAN or TCP-IP to the DCS-PCs. For more details on the DCS hardware see [2].

BASIC SOFTWARE

Following the LHC wide standard all our control software is developed using PVSS (Prozess-Visualisierungs- und SteuerungsSystem) a commercial product provided by ETM (Eisenstadt, Austria). Its concept is based on user defined data-point structures and managers, dedicated processes responsible for specific tasks. Our software is organized in three layers, the FIT (Front end Integration Tool), the SIT (System Integration Tool), and the FSM (Finite State Machine).

The bottom layer, the FIT, establishes the communication to the different hardware units. It reads the values from the hardware into data structures which follow the properties of the hardware devices.

The System Integration Tool provides the mapping between the hardware and the detector which is the fundament for the FSM. For all channels used in the mapping, the SIT initializes the archiving to the conditions database. To ensure a coherent operation of DCS and DAQ the actual mapping between hardware channels and detector is stored in the connectivity database, which is read by the DAQ and the SIT.

Using the distributed system mechanism of PVSS, our DCS software is split onto eleven control stations. While seven computers are mainly running the FIT projects, three machines handle the major parts of the FSM. The sub detector control station collects the information from all other machines and provides the interface to the shifter and central ATLAS DCS.

FINITE STATE MACHINE

While FIT and SIT are invisible for the normal user, the top layer of the DCS software, the FSM, is the tool to operate the detector. It allows for changes of the detector's operation mode in a simple but safe way and provides an overview on the detector status. Following an ATLAS wide decision we use the framework component 'controls hierarchy' [3]. To build the FSM, its structure, objects, states, and commands must be defined.

Tree of the Pixel Detector FSM

The FSM tree of the pixel detector is outlined as shown in Fig. 2. As required by ATLAS DCS the sub detector node PIX is composed of the DAQ partitions and an INF object which summarizes all infrastructure units: the optoheaters, the interlock system, the DAQ hardware, the DCS crates, the environment, the common infrastructure control of the racks and the evaporative cooling system. While the last two are just references to external systems

and are not under pixel control, the other infrastructure objects are pixel detector specific. Their internal branches are not shown here, see [4] for more details.

The further segmentation of the detector FSM follows the mechanical structure of the detector. Of major importance are the cooling circuits. In the case of Layer1 there are 19 cooling circuits, respectively bi-staves. Each bi-stave consists of four readout groups. These comprise the device units, which provide the actual connection to the hardware: the HV and LVs, one optoboard and the six or seven detector modules. The device units are rather complex themselves, e.g. the module combines the temperature and two LV channels of that individual detector element. As actually each command to the readout group can be a complex sequence of several operations, a special device unit, CMD, takes care of the synchronization of all steps and ensures that all sub-channels are handled in the correct order.

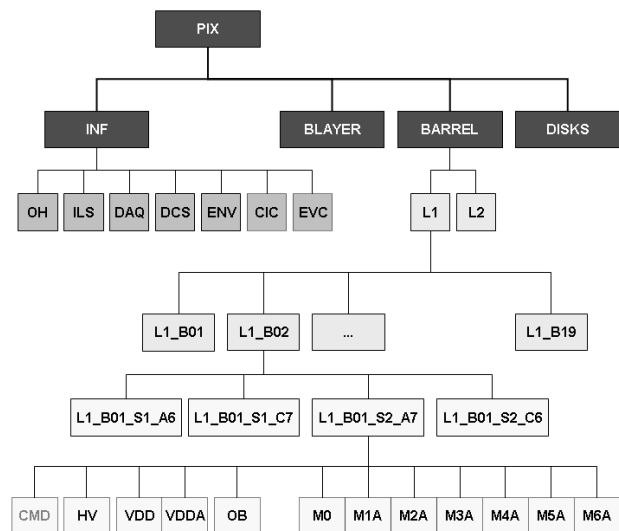


Figure 2: The FSM tree.

State Diagram of the Readout Group

The operation of the pixel detector is based on the control of the readout group. Its states and commands, which allow for the transition from one state to another, can be seen in Fig. 3. First the start-up procedure brings the hardware into a defined state (STARTED), followed by the switch on of the optoboards (OPTO_ON), of the LV (LV_ON) and finally of the HV (ON). The state READY can only be reached passively, when the DAQ has configured the front end chips. Whether the configuration was successful can be immediately seen by the current consumption of the readout chips. Additional states are introduced for special operations or situations. The state STANDBY protects against instable beam conditions. In this case the readout electronics stays powered, however the HV is ramped down. Additionally a special configuration is necessary to reduce noise and thus the state can not be reached without a DAQ action.

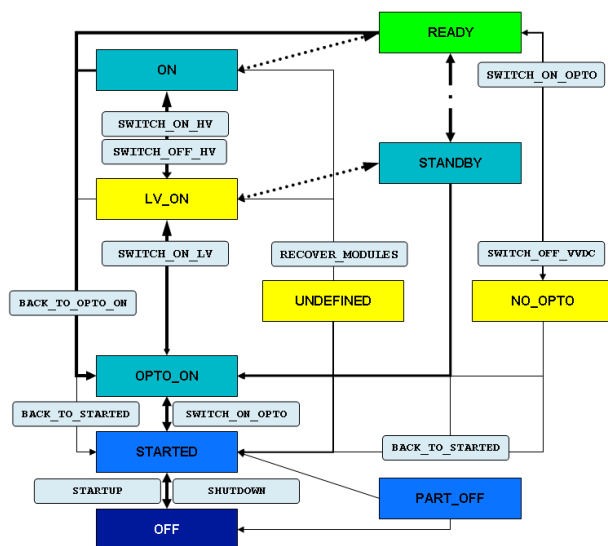


Figure 3: State diagram for the Readout Unit.

Software Interlocks

While the normal operation is performed by the shifter, critical situations are handled by automatic scripts. In case of high temperatures or exceptional current consumption of the modules or optoboards, the safety of the detector is affected. The hardware interlock system guarantees protection, but additional software interlocks make it possible to preemptively ramp down the power in a more controlled and synchronized way.

Interaction with Cooling System

The operation of the pixel detector and of the cooling system are strongly depending on each other. While it is immediately obvious that the pixel detector must be protected against overheating, and therefore can not be operated stably without cooling, on the other hand also the cooling system is dependent on the power dissipated by the detector as a heat load.

Therefore the startup of the two systems has to happen in a synchronized way, which is achieved by a handshake protocol between the two projects. This guarantees a fast and efficient startup of both systems.

A permanent monitoring of the cooling system ensures that all affected pixel equipment is switched off as soon as the corresponding part of the cooling system is not operational. As this is a safety relevant issue, it is completely automated and does not require any human intervention.

Scans of the Optical Link

The ATLAS DDC (DAQ DCS communication) package [5] provides a way of communicating data, messages, and commands between PVSS based DCS projects and the ATLAS DAQ online software. Currently the main use of DDC in the Pixel Detector consists in the support of special scans performed by the DAQ for the tuning of the optical link.

The most basic optical scan, the Inlink scan, is verifying the transmission of light from off detector to the optoboard, and needs to read DCS values for this. In case the pixel modules are powered during this scan, special care must be taken that they stay in a stable state by putting the optoboard into the NO_OPTO state (which stands for “no opto power”) with the dedicated SWITCH_OFF_VVDC command.

One of the values which is optimized by the BOC tuning is a voltage which is controlled and set by DCS. During the scan this value must be changed driven by the DAQ, and in subsequent operation the optimal value determined by the scan must be used. The pixel specific implementation of DDC provides a dedicated command for this task, thus enabling the DAQ to tune this value.

System Monitoring

An important aspect is the monitoring of the health of DCS itself. For this purpose, in every front end project, watchdog scripts monitor special heartbeat/alive items for each node. The monitoring of critical scripts and managers is done by the System Overview Tool, which was adapted from the JCOP framework package [6] for our needs. These tools complement each other as they are relying on different communication methods.

SUMMARY AND OUTLOOK

The ATLAS pixel detector requires for its operation a complex control system. The various aspects of monitoring, supplying the electronics with the required voltages, and safety must be covered. Using PVSS, a control system was developed which handles more than thirteen thousand individual control and monitoring channels. The operation of the pixel detector is performed with a finite state machine. It is closely related to the operation of both cooling system and DAQ. Various scripts monitoring and interacting with the cooling system ensure the safety of the detector and efficient common operation. The close relation to the DAQ is reflected in the state diagram of the FSM and special commands which support the tuning of the optical link. During the commissioning of the detector, the control system was used intensively, and was itself successfully proven to be adequate to the task of detector operation. An expert system, which will provide the operator with additional support to solve emerging problems, is in preparation.

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