RECONFIGURABLE DATA ACQUISITION SYSTEM FOR TIME RESOLVED MEASUREMENTS IN MULTIBUNCH MODE AT THE SLS

T. Korhonen, B. Kalantari, A. Puzic, J. Raabe, C. Quitmann,
Paul Scherrer Institut, CH-5232 Villigen, Switzerland

Abstract

The concept and the first implementation of a multichannel acquisition scheme handling 500 MHz data rate are presented. The input signal is generated by a fast photo detector which can resolve the time structure of the synchrotron and allows for single photon detection. The measurement of the electronic pulses coming from the detector is done with an ADC operating at 500 MS/s sampling rate. Dedicated timing hardware provides the synchronization of the entire setup with the storage ring. Custom counting logics is implemented using a fully reconfigurable FPGA. Low level device drivers and communication protocols are based on the VME standard and the EPICS toolkit. A processor core embedded in the FPGA controls the ADC settings and all the tasks of data transfer between the counters and the Input/Output Controller (IOC). The capability of the acquisition system is demonstrated by measurements of magnetization dynamics with the Scanning Transmission X-ray Microscope (STXM) at the Swiss Light Source (SLS).

INTRODUCTION

Pulsed time structure of electron storage ring results in an inherent time resolution of 50-100 ps. This value is mainly given by the width of individual electron *bunches*, which corresponds to the duration of photon flashes that are radiated when the path of relativistic electrons is bent by a magnetic field. Most experiments require only a very narrow bandwidth of synchrotron radiation spectra. Single flashes of these monochromatic photons have low intensity which inhibits "one-shot" measurements. Therefore, time-resolved experiments have to be performed in a stroboscopic way, accumulating the measuring signal over time periods considerably longer than the duration of the effect of interest. In the commonly used *pump-probe* arrangement the specimen is excited by a *pump* pulse at the time $t = 0$ and a photon flash generated by the synchrotron *probes* its state at a defined delay time step Δt. This sequence is repeated and the measuring signal is integrated until the necessary signal-to-noise ratio (SNR) is reached. The repetition rate of the pump pulses depends on the intrinsic relaxation time of the investigated sample. Dynamic response is measured by increasing the relative delay time of the probing flashes in multiples of Δt until the sample reaches equilibrium. At the SLS, individual bunches arrive with a period of ≈ 2 ns due to the accelerating RF of ≈ 500 MHz. Two subsequent photon flashes probe two sample states which are 2 ns apart. The detection and the signal processing have to be sufficiently sensitive and fast in order to distinguish these two states from one another. In many experiments two-dimensional detectors like CCD sensors are used which cannot be read out that fast because of the large number of pixels. For this case, storage rings operate in special modes for time-resolved measurements or, like at the SLS, a high intensity *camshaft* bunch in the gap of the filling pattern is provided. The gap width of 180 ns facilitates gating of the detector during the *multibunch* train while the sample is probed only with the isolated photon pulse [1].

Here we present a different approach, which enables the detection and signal processing at 500 MHz data rate. The detection scheme relies on a fast point-detector which can resolve the time structure of the SLS and allows for fast electronic read-out. With a dedicated data acquisition board one is able to continuously distribute the signals originating from the consecutive dynamic sample states, which are 2 ns apart, into different counters and to use the full photon flux in the top-up multibunch operation mode. Utilizing this flexible concept, various timing configurations are possible in order to meet different requirements of individual time-resolved experiments [2].

CONCEPT AND REALIZATION

The concept for the data acquisition system is based on fast detection of single (or multiple) events and their subsequent synchronous distribution and counting. The development is motivated by the demand for measurements of photon intensity with high time resolution at several experimental stations of the SLS. Such measurements are needed mainly for time-resolved experiments where photons have to be detected after their interaction with a specimen. Furthermore, they can also be used for purposes of diagnostics or as a reference for the scaling of measurement data. By taking into account all the requirements from different beamlines, we made a collection of features which should be implemented in a multichannel data acquisition system:

- full mapping of the SLS filling pattern
- gating of empty buckets and the camshaft; routing of distinct bunches into dedicated counters
- option for different routing schemes per full revolution of the filling in the storage ting
- timing reference and trigger signals for diagnostics and synchronization of excitation electronics
- the acquisition system has to be easily reconfigurable and adaptable to different experimental requirements.

In this paper we describe a particular realization for the STXM at the PolLux beamline, operating in the soft X-ray region of the electromagnetic spectrum [3]. The conceptual block scheme is shown in Figure 1.

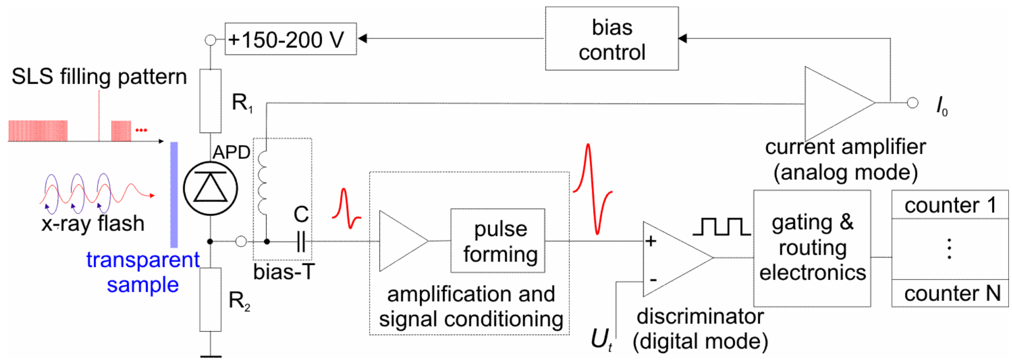

Figure 1: Conceptual block scheme for time-resolved measurements in *multibunch* mode.

Off-the-shelf avalanche photodiodes (APD) are capable of direct X-ray detection with single photon sensitivity [4]. They exhibit high SNR due to the internal amplification. For the photon counting application at the STXM we have chosen APDs with a fast time response combined with active areas that match the optical arrangement of the microscope [5, 6]. The average flux at the sample site amounts to approximately one photon per bunch, which makes the concept of *single photon counting* straightforward. After the amplification and conditioning of the APD signal, bipolar electronic pulses with peak amplitudes of 50-100 mV and duration of 400-600 ps are presented to the counting electronics. At the STXM, the counter values correspond to the beam intensity transmitted through the sample.

PRESENT STATUS AND FUTURE DEVELOPMENTS

The implementation of the acquisition system is done with a custom data acquisition card, featuring two dual-channel, 8-bit ADCs with a maximum sampling rate of 1 GS/s and two Virtex-II Pro FPGAs [7]. One FPGA is used as an event receiver (EVR-FPGA) which recovers the storage ring RF and derives other timing and triggering signals from the global event distribution system, like the ring revolution clock (RF/480 = 1.042 MHz), the synchronization for electronic signal generators and pulsers (RF/50 ≈ 10 MHz) and the signal for the gating of the top-up injections occurring every 3 minutes [8, 9]. The EVR-FPGA provides access to the VME bus, as well as connections to the Ethernet and the RS232 debugging port. The acquisition and processing of the data sampled by the ADCs is implemented in the second DAQ-FPGA. The two FPGAs communicate via RocketIO links. Embedded PowerPC processor controls the ADC setting and manages the communication with internal and external busses and ports. Figure 2 shows the overview of main hardware and software parts of the entire system. The distribution discrimination and counting of the APD pulses has to occur synchronously with the storage ring.

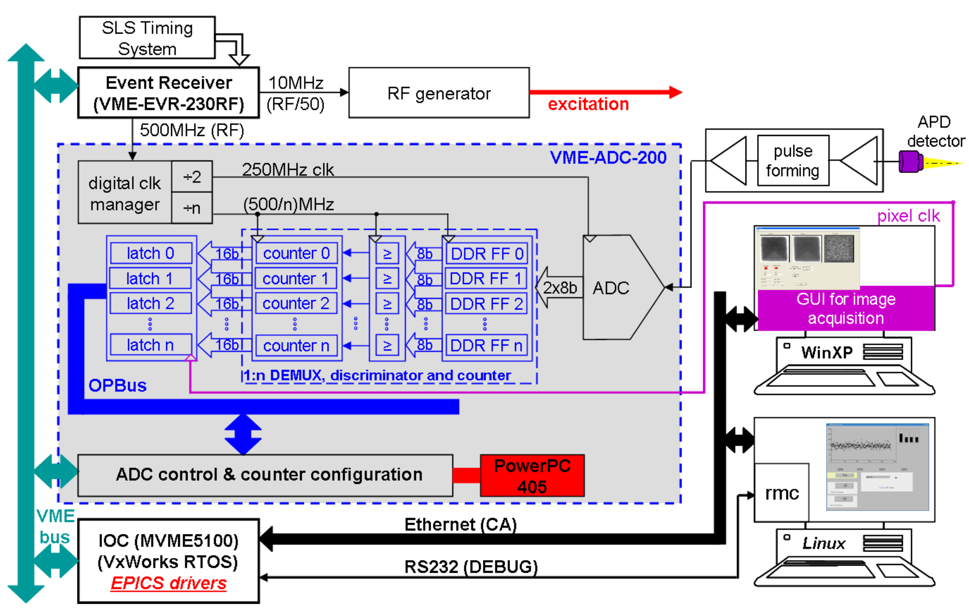

Figure 2: Main hardware and software components of the synchronous multichannel data acquisition system.

Therefore, a digital clock manager in the DAQ-FPGA regenerates the clock from the RF and provides all the necessary sub-clocks. The ADC conversion clock is set to RF frequency and the sampling rate of 500 MS/s is sufficient for this particular implementation. The ADC delivers two 8-bit samples every clock period. Double data rate flip-flops (DDR-FF) are used to distribute the samples, which are subsequently discriminated to 1-bit (1 or 0, depending on the pulse height relative to discriminator threshold). The counters that are defined in the firmware as 16-bit registers add up the values coming from the discriminator. The raw samples are also stored in a Block RAM to enable tuning of the sampling phase and the discriminator level setting. The clocking of the digital signal chain is strictly related to the number of counter channels.

The signal that starts and stops the counters and the data transfer is provided by the PC which controls the scanning stage of the STXM. This is the only asynchronous signal in the system and has to be "re-sampled" in the FPGA. Its duration corresponds to the dwell time for a single pixel and is equivalent to the total counting time. When "*pixel clock*" changes to low, the counter values are latched and read into EPICS channels. The Channel Access protocol (CA) is then used to transfer the data further to the Graphical User Interface (GUI) for image acquisition, running an the STXM control PC. This GUI is programmed using LabWindows software package.

The performance of the system was demonstrated by time-resolved imaging of magnetization dynamics in ferromagnetic microstructures. The images in Figure 3 show snapshots of the magnetization at two phases of the gyrotropic vortex motion [10] in the cobalt layer of the trilayer stack $Ni_{80}Fe_{20}$(40 nm) / Cu(2.8 nm) / Co(40 nm). The sample with lateral dimensions of 1.5 µm × 1.5 µm is excited by magnetic induction alternating at the frequency of 250 MHz with amplitude of 2 mT.

Initial tests were performed in the low-α operation mode of the SLS (mean electron beam current of 50 mA, temporal width of photon flashes: 5-10 ps). The detection and the data acquisition schemes accommodate lower measurement signals due to the sensitivity and high SNR of the photon counting technique. This opens new possibilities for time-resolved experiments with up to ten times higher temporal resolution, compared to the normal operation mode of the SLS.

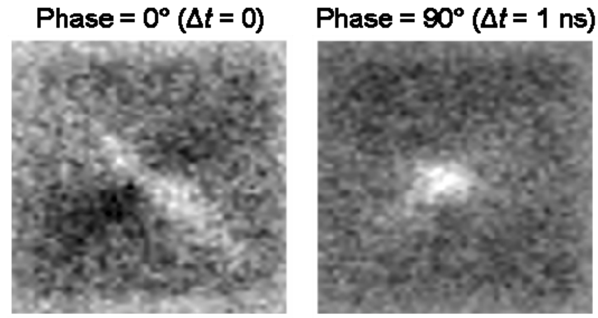

Figure 3: First time-resolved measurements of magnetization dynamics in multibunch mode at the SLS.

Currently, the system is running synchronized to RF but with an arbitrary phase relation relative to the revolution clock of the SLS. The data acquisition will be additionally synchronized with this clock, in order to implement the remaining features of the basic functionality, like the gating of the empty buckets and the camshaft, or different routing schemes per ring revolution. The counters will be extended to 32-bit width and the number of them will be increased accordingly to enable the implementation of a flexible bucket gating scheme. Consequently, the EPICS drivers and the image acquisition GUI have to be extended for the possibility of user-friendly reconfiguration and control of the data acquisition system.

REFERENCES

[1] C. Quitmann et al., Nucl. Instrum. Meth. Phys. Res. A, 588, 494, (2008).
[2] Y. Acremann et al., Rev. Sci. Instrum. 78, 014702 (2007).
[3] J. Raabe et al., Rev. Sci. Instrum. 79, 113704 (2008).
[4] A. Q. R. Baron et al., J. Synchrotron Rad. 13, 131-142 (2006).
[5] Hamamatsu, Si APD: models S2381 and S2382; http://www.hamamatsu.de.
[6] Silicon Sensor GmbH, models AD230-8 and AD500-8; http://www.silicon-sensor.com/.
[7] VME-ADC-200, Micro-Research Finland Oy; this card was initially designed for the Filling Pattern Feedback System at the SLS. http://www.mrf.fi/.
[8] T. Korhonen et al., Proceedings of ICALEPCS2001, San Jose, California.
[9] B. Kalantari et al., Proceedings of ICALEPCS2003, Gyeongju, Korea.
[10] A. Puzic et al., J. App. Phys. 97, 10E704 (2005).