THE CONTROL SYSTEM FOR INDUCTION ACCELERATION IN THE KEK DIGITAL ACCELERATOR

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Abstract

A digital accelerator (DA) is a low energy version of the induction synchrotron which has been demonstrated using the KEK 12 GeV-PS in 2006. In the DA of injector-free, the acceleration and bunch confinement are independently carried out by induction cells, which are 1-to-1 transformers driven by individual switching power supplies. The switching power supply employing high power semiconductor switching devices (MOS-FET) can be operated at an arbitrary repetition rate up to 1 MHz with an output voltage of 2 kV. This characteristic allows us to realize a so-called all-ion accelerator capable of accelerating all species of ion including cluster ions. To comply with specific demands for the induction acceleration in the KEK DA, that is a renovation of the existing KEK 500 MeV Booster synchrotron, a fully digital control system of the KEK DA is under development. It consists of high speed ADCs and FPGA (or DSP) to acquire the profile of beam bunch and process the required gate trigger signal from the profile data. It is crucial to trigger the acceleration system at the desired timing. Outline and R&D works of the control system are described.

INTRODUCTION

The all-ion accelerator (AIA) is one example of the application of the induction synchrotron, which was proposed by Takayama and Kishiro in 2000 and fully demonstrated by using the KEK 12GeV proton synchrotron (PS) in 2006 [1]. Ions in the induction synchrotron are accelerated and captured with pulse voltages generated by transformers (induction acceleration cell, IC). The transformer is energized by the corresponding switching power supply (SPS), in which power solid-state conductors are employed as switching elements and their tuning on/off are switched by gate signals digitally manipulated from the circulating signal of an ion beam. Consequently, the acceleration is always synchronized with the revolution of the ion beam irrespective of the charge state of the ion. Thus, any ion directly injected from an ion source can be accelerated from extremely low velocities to nearly light velocity. In other words, the IC is free from the limitation of bandwidth of the acceleration cavities or the limitation of the amplifier which is commonly used in conventional rf synchrotrons. This ability to accelerate particles of arbitrary charge and mass is the main concept of the AIA, which is hereafter called a digital accelerator. At present the KEK 500 MeV booster, which has been utilized as an injector for the KEK 12GeV PS for over 30 years, is under renovation to be transformed into the first digital accelerator (KEK-DA) in the world. The KEK-DA is a rapid cycling synchrotron, in which the accelerating voltage per turn is rapidly varied from 0V to 2.4kV and to then to 0V through the acceleration period, and the revolution frequency at the end of acceleration is of the order of several megahertz because of a small ring area. Such characteristics of the accelerator demand novel operations of the induction acceleration system that have not been realized in the proof of principle experiment of the induction synchrotron. At present, 10 induction cells with a fixed output voltage of 2kV and with the capability of being operated at a maximum switching frequency of 1MHz are available.

In this presentation the present control system and the future plan of advanced digital signal processing method are explained.

KEK-DA

Figure 1 shows the schematic diagram of the KEK-DA [2]. The induction acceleration system consists of ICs, SPSs, DC power supplies (DCPS) for the SPSs, and the gate control system to drive the SPSs. Most of the ICs, SPSs, and DCPSs have been used to experimentally prove the concept of our induction synchrotron. These devices will be installed in the former 40MeV linac, and the booster ring area. Futhermore, the 9.4GHz Electron Cyclotron Resonance (ECR) ion source is being tested for implementation. In the first stage of the KEK-DA, argon ions are assumed to be accelerated. Ar ions generated in the ECR ion source embedded in a 200kV high-voltage terminal are injected into the KEK-DA through a short low-energy beam line placed after the momentum separator. The KEK-DA is a combined-type FDFO lattice. Two existing RF cavities, which occupy two straight sections, are replaced by 9 induction cells. At present, the power supply systems for the main magnets and evacuation system are being renovated.

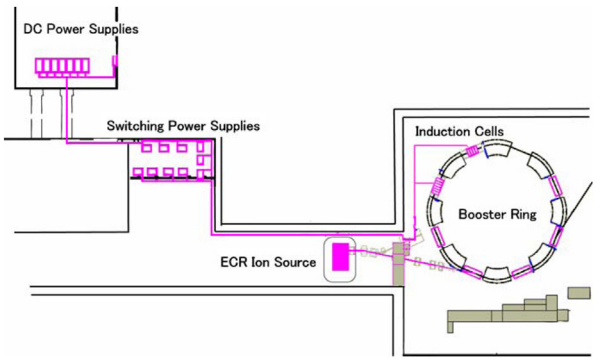

Figure 1: The outline of KEK-DA.

DA CONTROL SYSTEM

Present Control System

In the KEK-DA induction timing is very important, therefore, the beam velocity and the passing time through the bunch monitor are required to calculate the arrival time at the induction cell to produce induction field to synchronize the bunch of particles.

In the present system to realize the requirements a bunch monitor is used to estimate the induction timing using digital signal processors (DSPs). Based on the time-scheme of magnetic field strength, the confined beam velocity can be exactly calculated by beam traveling time. From the derived beam velocity and the distance between the bunch monitor and the induction cell the induction timing can be determined.

Figure 2 shows an example of the voltage scheme of two induction cells. During the positive period the passing particles are accelerated. The front and back negative portions are inevitably combined with positive portion because the polarity of the electromotive force alternately must change. As shown in Fig. 3 the timing and the width of these four divisions are controlled by eight individual separate timing pulses originated from eight DSPs. Each DSP receives a common trigger pulse from the bunch monitor and starts to calculate each delay time to output each timing pulse to start or stop the coil current of induction cells. The timing varies as the beam velocity increases.

DSP

In the present system the digital signal processors (DSPs) manufactured by Texas Instruments Co. Ltd are used for the core of the intelligent trigger system. The DSP (DSK6416T) can be programmed using the C-language; it has 32-bit timers with a clock frequency of 128MHz. Futherrmore, the processor has analog/digital converters to process analog inputs. The program obtains timing information from the ramping pattern of the bending magnets and calculates the necessary delay time. The delay time for each turn is set on the timers when the program is interrupted by beam-bunch signals.

In the KEK-DA, a so-called ΔR feedback system is included. The ΔR means the difference position from the ideal orbit. The orbit information proportional to the momentum error is processed in the DSP and when ΔR exceeds the threshold value, the acceleration voltage is turned off. In this way, the over speed of particles is suppressed by the ΔR feedback system.

Advanced Control System

Though the present control system is easy to change software to modify the control method, the eight DSP board sets are large enough to a 19 inch rack. Therefore we considered an advanced control system. It consists of only a Field Programmable Gate Array (FPGA). Table.1 shows the merits and the demerits of the present control system and the advanced control system. As shown in Fig. 4 the FPGA outputs four digital signals for coil currents. The first pair of blue signals is for the first cell. The second pair of orange signals is for the second cell.

The system becomes very compact and its processing time will be improved by parallel processing and arithmetical computation technique using lookup table memories.

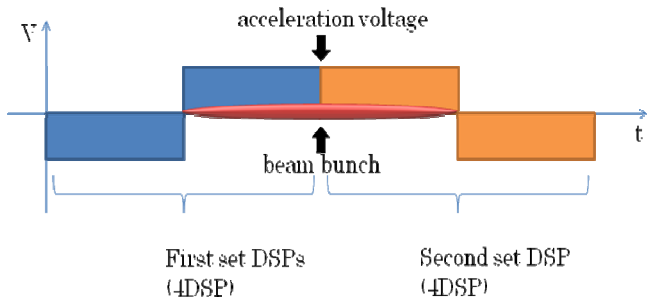

Figure 2: The relation between voltage of the IC and time in the position of the IC.

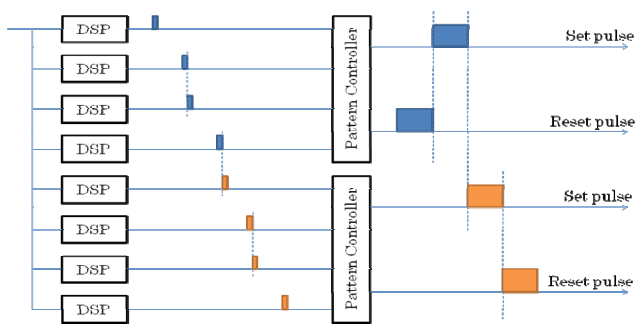

Figure 3: The control IC of DSPs of two set.

Table 1: Merit and Demerit of Current Control Method and Suggestion Control Method

Control Method	Merit	Demerit
Suggestion	Speedup Parallel Resources saving	Not general Understanding of the hardware
Current	The degree of freedom of the program	Overspec

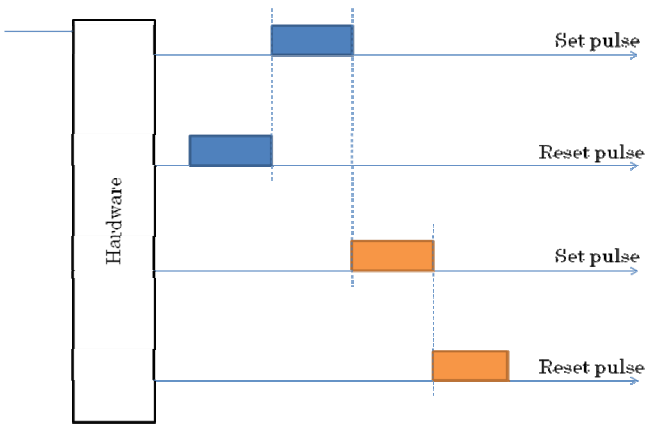

Figure 4: The block diagram which make hardware.

In the present system eight DSPs are executing same program individually loaded by a computer and the DSPs can not communicate each other. Therefore, the loading all processing units into single FPGA hardware circuit is very effective to scale down the control system and the system is easy to change the operating parameters.

FUTURE DEVELOPMENTS

- To select an evaluation board implemented by an appropriate Xilinx FPGA device and install Verilog HDL program developed by ISE foundation.
- To make simulation test using a pulse generator.
- compare the performance with the present system.

REFERENCES

[1] Ken Takayama, Yosio Arakida, Tanuja Dixit, Taiki Iwashita, Tadaaki Kono, Eiji Nakamura, Kazunori Otsuka, Yoshito Shimosaki, Kota Torikai, and Masayoshi Wake, PRL 98, 054801 (2007).

[2] Taiki Iwashita, Yoshio Arakida, Tadaaki Kono, Ken Takayama, Tanuja Dixit, A 606 (2009) 111-115.