CONTROL ARCHITECTURE OF A NEW PSU CONTROLLER FOR DIAMOND LIGHT SOURCE

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Abstract

A new magnet power supply controller is currently being designed for Diamond Light Source. The design uses digital regulation implemented in an FPGA. An embedded ARM processor is used to provide integration with the supervisory control system. Interfaces are also provided for integration with the fast orbit feed back system and for synchronous control of multiple supplies. Details of the architecture and progress in the realization will be presented.

INTRODUCTION

Diamond, a third generation 3GeV synchrotron light source[1], commenced operation in January 2007. The storage ring (SR) is based on a 24-cell double bend achromatic lattice of 561m circumference. It uses a full-energy booster synchrotron and a Linac for injection. The current operational state includes twelve photon beamlines and experimental stations, with a further nine beamlines now under design or construction.

Diamond uses approximately 1200 DC power supplies to energise electromagnets. These range in power from tens of watts, for corrector magnets, to 750kW for the storage ring dipoles[2, 3]. All power converters are controlled using a common design of digital PSU controller which was developed at the Paul Scherrer Institut (PSI) for the Swiss Light Source[4]. This solution has provided excellent standardisation and optimal reliability on Diamond. However, the PSI design is now suffering from component obsolescence; hence a new design providing similar levels of functionality but with improved performance is being developed. The new design further simplifies integration into the overall control system by including sufficient computing resource to support running an EPICS control system server directly connected to the control system network.

This paper presents the design for the Diamond Power Supply Controller (DPSC), and reports on progress to date. Analysis of the performance of this design is currently ongoing and will be the subject of a future publication.

OVERVIEW OF THE DESIGN

The DPSC provides closed loop-control of the PSU, providing the regulation of the power electronics to achieve the required performance together with state-based control and interlocking for correct operation of the PSU. The design is intended for, but not limited to, Switch Mode power supplies where the power electronics are controlled through a PWM signal and the output current is measured using a DCCT or burden resistor and is returned as an analogue signal. The realisation is based on an Xilinx FPGA, one 24-bit ADC, four 16-bit ADCs, four 16-bit DACs, a USB interface, FLASH and RAM memory, and a DIMM based processor board. It is realised as a Eurocard module and is mechanically compatible with the PSI controller.

Figure 1: Diamond Power Supply Controller.

It provides the following interfaces as show in Figure 2:

- 100Mbit Ethernet: To the Control System;
- USB: For local control console;
- 100Mbit Ethernet: Direct to the FPGA for low latency data for feedback applications;
- Optical Signal: Timing signal for synchronisation;
- Analogue Outputs: From four 16-bit DACs for oscilloscope based monitoring;
- Analogue Inputs: To four 16-bit ADCs for secondary control loop and monitoring;
- Analogue Input: To a 24-bit ADC for main control loop;
- Digital Output: PWM signal for driving inverter modules;
- Digital IO: For communications and synchronisation with other modules in a master slave mode.

FPGA FUNCTIONALITY

The DPSC uses a single Xilinx Spartan-3E FPGA for all logic communications and signal processing. The principal

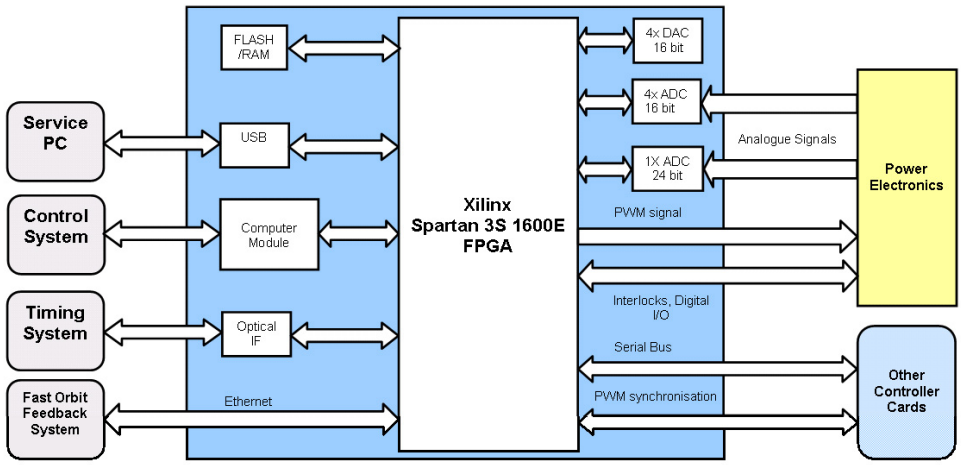

Figure 2: Block diagram of Diamond Power Supply Controller.

modules realising this are: Feedback Controller & State Machine, PWM Generator, Communications Interface, Processor Board Interface and a Virtual Scope. Each of these modules is described below.

Feedback Controller & State Machine

The feedback controller manages the signal processing from the 24-bit ADC interface used to read digitised magnet current signal, to the PWM output. The module uses data from a 4 channel 16-bit ADC interface block for monitoring DC link and output voltages, and drives a 4 channel DAC with 16 user selectable signals from the feedback process. It also controls 8 isolated digital outputs.

The State Machine manages internal and external interlocks, from the 16 isolated digital inputs, to ensure the correct operation of the DPSC.

The Feedback Controller & State Machine module is programmed using Xilink toolbox in Matlab/Simulink, and then embedded into the top-level VHDL design.

PWM Generator

Figure 3 shows Slow Corrector PWM waveform signals (S0 and S1). The time resolution of the PWM signals is enhanced by using the FPGA's ability to phase shift its clock combined with a recursive algorithm to quantise the fractions of the clock cycle required for the PWM signal.

The PWM signals are generated according to Equations 1 and 2.

$$t_1 = no\_clks + ph\_clk * (90/n * 360 * f_{clk}) \quad (1)$$

$$\tau = (250 - t_1)/2 \quad (2)$$

where ph_clk is the phase step of the reference clock (0..3), and no_clk is the pwm pulse length in terms of clock cycles.

With a 50MHz reference clock, this provides a time resolution of 5 ns. The recursive algorithm dithers the PWM output signals between time steps.

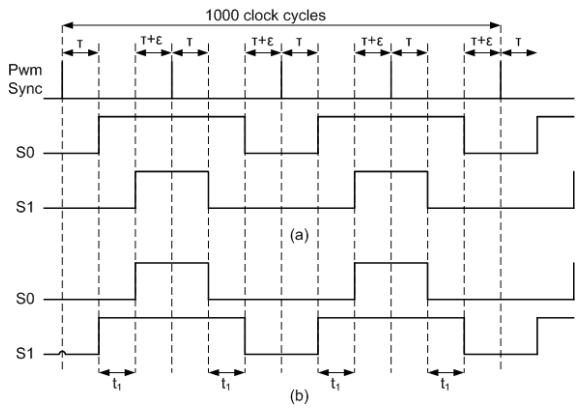

Figure 3: Slow controller PWM output signals for (a) $m > 0$, (b) $m < 0$, where m is the modulation index.

Communications Interface

The Communications Interface module manages all the communications between PCView[5], which is a LabView application running on a local service PC, and external peripherals via FPGA. An 8-bit PicoBlaze processor embedded in the FPGA works as a communication controller interfacing the following devices:

- USB Transceiver : The interface to a local PC is over a USB connection.
- Flash : A 64M Flash is used to store DPSC parameters and waveform values.
- DDR SDRAM : An external DDR SDRAM is used for storing hit values in ADC calibration mode and storing ADC linearity correction values in normal operation.
- Processor Board : The control system interface is handled by EPICS running on the processor board.

The DPSC operation is controlled and monitored using four sets of parameter space including:

Monitored Signals: Signals such as the State Machine State, alarms, output current and voltage etc are regularly sampled and transmitted to PCView.

Communication Registers: Operator set parameters such as the current reference and On/Off commands are written to communications registers.

Parameters: Parameters are stored in Flash memory and are loaded into the Parameter Registers on power up; they can also be read from and written to Flash memory. When parameters are changed the Setting Up bit is cleared; this sends the State Machine to its PC Tripped state to ensure the power converter is shut down while they are changing. The Setting Up bit is set when the new parameters are loaded.

Waveforms: A single waveform is stored in Flash memory. It is read out when requested by the Waveform Reference block. Waveforms can be read and written to using PCView.

Processor Board Interface

The processor board interface provides an asynchronous interface between Single Board Computer and FPGA design register space. The register space is composed of control and status registers, and the interface to processor board is provided through receive and transmit FIFOs. Each FIFO is 256×8-bit wide and has the same data structure interface to Picoblaze as the USB interface.

Virtual Scope

A 512x32-bit BlockRAM is used in order to store 128 samples from each of four data channels. Virtual Scope can run in two modes called Free Run Mode and Triggered Mode. In Free Run mode samples are taken at the rate determined by the sample interval, then read out to PCView. Once this cycle is complete it is repeated. In Triggered Mode, sampling is continuous at a rate determined by the sample interval, until a trigger condition is met. *N* samples are then taken and the result read out to PCView. Triggering occurs when two successive samples with the right slope exceed the trigger level.

PROCESSOR BOARD

The DPSC is designed to run with an optional integrated control system interface. In the case of Diamond this is based on the EPICS Controls System toolkit, but integration of other control systems should also be possible. The EPICS IOC (IO Controller) runs on an embedded processor board, the "Colibri"[6]. This module integrates an ARM XScale processor (running at 312 MHz or 520 MHz), 32MB flash, 64MB RAM and a 100 Mbit Ethernet controller into a module measuring 68mm x 37mm that fits into a standard SO-DIMM socket.

The connector to the Colibri module exposes the processor interface with little or no intermediate circuitry: all integrated processor GPIO pins are available, together with the full address and data bus. This application uses only the data bus, a chip select and a few address pins together with interrupts to the FPGA, allocates some GPIO pins for programming the FPGA, and brings out the Ethernet interface and serial port for communication.

The Linux kernel supports the Colibri modules using a standard build of the kernel with minimal patching. The compiler tool chain and C library were built using the excellent crosstool-NG[7] project, which easily allows cross compilers and libraries to be built and kept up-to-date. The software chain on this processor comprises: the "u-boot" boot loader, the Linux kernel, the GNU C run time library, Busybox for the boot and command line environment, Dropbear for secure shell, the reference NTP server for accurate timestamping, and EPICS. With a little care it is easy to fit a complete Linux system built using these tools into the 6MB of memory. Thus the environment provided by the Colibri module is more than adequate. The resulting environment is almost identical to that used in the Libera Electron Beam Position monitor, with which Diamond has considerable experience, so that the same EPICS build is used on both processors[8].

PROGRESS AND FUTURE PLANS

Current progress in the DPSC is that the hardware has been used to control a small power supply in laboratory. Using this, characterisation and validation of the performance is currently being undertaken. There also remains work to realise some aspects of the control and monitoring functions and the overall control system integration. Following on from this a number of the controllers will be deployed on Diamond to establish its long term reliability.

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