FPGA DIGITAL TIMING SYSTEM FOR FUSION PLASMA DIAGNOSTICS IN LHD

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Abstract

The digital timing system for LHD diagnostics was developed more than ten years ago as a VMEbus module which was operated by VxWorks RTOS. Through the fiber links, it can deliver the master trigger and the 10 MHz base clock which is modulated with the encoded trigger message. It has a simple tree structure from a master modulator to end demodulators whose output signal edges are all aligned to the delivered base clock. As the VME module and VxWorks were very costly to maintain, they have been ported into the new SoC platform, Xilinx Spartan-3E, that has 1.2 M programmable gates and Microblaze cpu which can run μClinux on it. Using its semi-finished commercial module Suzaku-S, the unit cost of a modulator box becomes one-eighth of previous VME one. In addition, it can output 6 delayed triggers, 6 divided clocks with their own (6) gating time, whereas VME provided 6-2-2. The same network communication schemes are completely implemented on uClinux, ported from the RPC source codes running on VxWorks. As such the semi-finished SoC platform is very useful to homemade an intelligent digitizer unit, another fast latching scaler module is now designed to be made for LHD (Large Helical Device).

INTRODUCTION

Generally speaking, fusion experiments have various kinds of high-temperature plasma diagnostic measurements [1]. Such the tendency becomes more obvious especially in larger experiments like LHD (Large Helical Device). To supply the various digitizers with their own start trigger and sampling clock independently, we developed the digitally synchronized timing delivery system (DTS) more than ten years ago [2, 3].

The diagnostic timing system for LHD fusion plasma measurements is a synchronous clock and trigger distribution mechanism whose tree-structured optical fiber links connect the single master modulator and terminal demodulators. As those modules were made based on VMEbus standard and running on VxWorks real-time operating system (RTOS), all the master and terminal nodes need their own cpu board, vme backplane and chassis. Their hardware and software maintenance or improvement, therefore, have needed high expenses including the development environment and license.

On the other hand, technical innovation of FPGA-based one-chip integrated system has been highly advanced and also widespread to such the physics research field recently. On a basis of the number of programmable logical units integrated within a FPGA chip, its growth is one thousandfold or so than ten years ago. Such the small but highly integrated computer system becomes very popular under the name of "system-on-a-chip (SoC)" nowadays.

Considering those surroundings, we have decided to develop an improved DTS module based on a new SoC platform. It is expected not only to reduce the production cost drastically but also to be more reliable like a maintenance-free black box.

DIAGNOSTIC TIMING SYSTEM OF LHD

LHD is well known by its enriched measurements in fusion experiments, holding the world record of acquisition data amount in one discharge, 90 GB. At the moment, it has more than 70 plasma measuring devices installed around the main body, even though their numbers of signal channels are several tens in average, usually no more than one hundred.

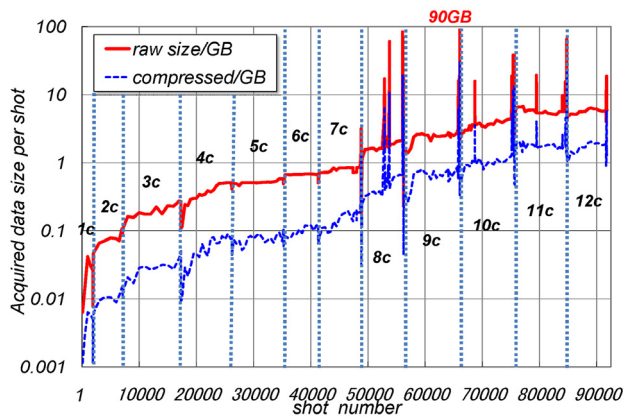

Figure 1: LHD's diagnostic data amount per shot: It has usually ∼170 discharge experiments, *i.e.* "shots", per day.

As every plasma diagnostics continuously observe time-evolutional plasma behaviors, eventual phase transitions, and fluctuation spectrum, namely "modes", all the sampling clocks and start-digitizing triggers should be synchronized precisely among the numbers of distributed diagnostic digitizers. In LHD, DTS delivers a 10 MHz base clock of the highly stabilized master oscillator to all the terminal DTS nodes in which programmable frequency dividers can output any preset frequencies divided by the base clock. Consequently any divided clocks will be perfectly in phase of the base clock's edges.

Start triggers for each measurement will be delivered upon the base clock modulated by an encoded message of

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the master trigger. Every trigger outputs of the terminal nodes have programmable delaying counters, and will demodulate the encoded master trigger to start counting for generating the delayed pulses. The whole structure is based on a simple *"modulator–demodulator"* scheme, as shown in Fig. 2.

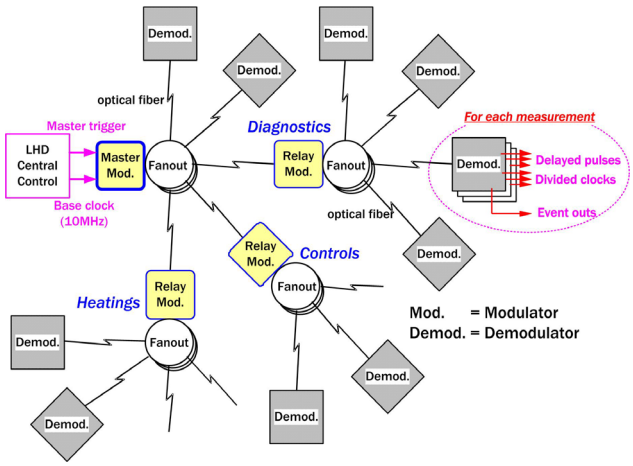

Figure 2: Schematic structure of DTS: The simple tree structure consists of a master modulator, relay modulator(s), terminal demodulator(s), and the optical fiber links between them.

For the practical use by grouping some terminal demodulators separately from others, a modulator can alternatively behave as the relaying one between the master and the terminal nodes. As multiple fiber links can be branched off, the optical fan-out modules are additionally applied especially for master and relay modulators. Such the capability to make a branch sub-structure and group the leaf nodes will provide a wide flexibility having multi-tier structure and therefore give the easy expandability to the system.

As shown in Figs. 3 and 4, DTS modulator and demodulator were made as VMEbus modules which had been running on VxWorks real-time operating system (RTOS). Each DTS module except the master modulator has one

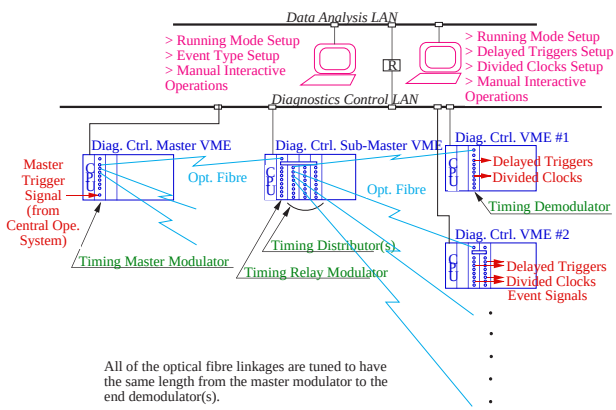

Figure 3: Physical connection view between DTS nodes and LAN communication links to the clients.

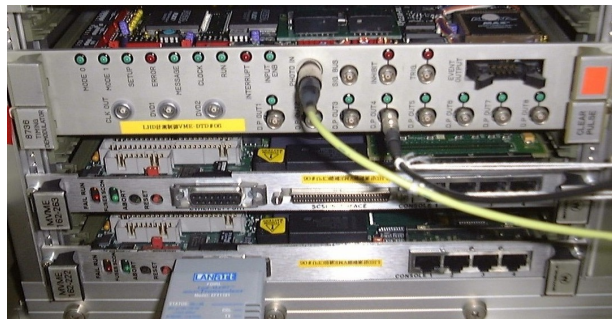

Figure 4: VME-based DTS system: two cpu boards and the demodulator in a vme chassis.

photo-in port to receive the modulated signal from the upstream node through an optical fiber. Preprogrammed triggers and divided clocks can be output only by the terminal demodulators to run digitizers.

NEW SoC-BASED IMPLEMENTATION

SoC Platform and Environment

The requested conditions for the new SoC-based implementation were considered as follows:

1. As DTS demodulator uses many 16 or 34 bit counters in logics, the required number of gates should be more than a million. Chip cost is another important issue.

2. To port the vme-based software easily, the SoC chip should include the cpu core inside on which some OS runs for executing the onc rpc server codes [4].

We have chosen Atmark Techno's semi-finished FPGA-based module "Suzaku-S (SZ130)", which has a 1.2 M gate Xilinx Spartan-3E FPGA chip on board and a software processor Microblaze can be embedded within it. As it costs only about us$ 300 having card-size (47×72 mm) dimensions, we have decided that it is quite suitable both in casing and mass use in LHD.

μCLinux, no-MMU linux kernel, can run so as to execute the rpc services there. As it is so-called the embedded OS kernel, it does not need the specific kernel driver developed for interfacing with FPGA user logics. For the IDE, ISE9.1i and EDK9.1i freely provided by Xilinx were used.

Logic and Circuit Design

The block diagram of the new FPGA demodulator is shown in Fig. 5. Except the base-clock extracting PLL and some i/o buffers, all the remaining circuits have been contained in "Suzaku-S" unit. User programmable FPGA area has been newly programmed in VHDL (VHSIC Hardware Description Language), even through the conceptual diagram was followed from the former VME one. The optical receiver, Nanahoshi's FCM-100M, was chosen through some compatibility tests with the modulator's optical transmitter, both of which have been already discontinued.

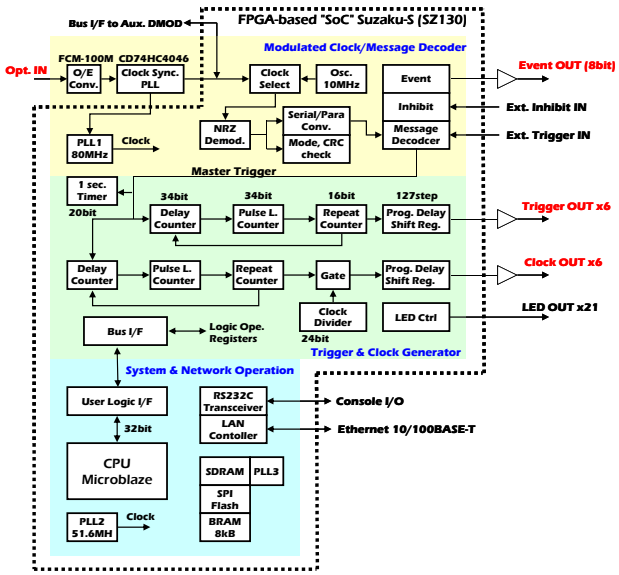

Figure 5: Block diagram of new SoC demodulator.

Base-clock extracting PLL is indispensable to make the demodulators' clock counters precisely in phase with the 10 MHz base clock from the master modulator. The delivered clock, however, is bi-phase encoded by timing messages and therefore cannot be used as the synchronous clock as it is. The PLL circuit is necessary to extract the original 10 MHz base clock properly. The locked clock is then used to decode the NRZ encoded messages which would start delayed trigger and divided clock counters.

It can alternatively change the clock source to the local oscillator in case of standalone execution or local tests without any optical signal.

Trigger and Clock Generators have their respective counters that start up-counting till the preset count reached and the comparator will then output the pulse(s). The tailing shift registers can delay the outputs with maximum 12.5 ns $\times$ 127 steps for compensating the difference of optical fiber lengths to every demodulators.

Embedded Micro-Computer is a software microprocessor "Microblaze" constructed on FPGA area, which provides some parameter setup and status monitoring services through Ethernet or RS-232C serial console, running on μCLinux OS. The communication between the cpu and the wired logics is enabled by the user-logic interface in cpu side and the 32-bit bus interface having 38 registers in logic side. The mutual data exchanges will be done through these registers.

First, we developed a prototype having eight triggers, clocks and the gated outputs. Then, the logics spent 80 $\sim$ 90 % of silicon resources in which the timing counters are widely arranged on logic area and therefore the cpu region was somewhat restricted. In such the situation, cpu could not boot at the optimal clock of 51.6 MHz.

To recover this problem in release model for practical use, we have lessen the number of implemented trigger and clock channels from 8 to 6, and also reduced the cpu clock from 51.6 MHz to 36.8 MHz for the stability margin. Though this time we used the automatic arrangement utility, more particular arrangements by hand might be expected for guaranteeing reliable behaviors of other parts and also realizing further optimization.

Figure 6: Front and inside view of newly developed FPGA demodulator box: The central small piggyback module is *Atmark Techno's Suzaku-S (SZ130)*.

CONCLUSION

The whole functionality provided by VME-based DTS hardware and the application software running on VxWorks have been completely implemented into a small "SoC" platform. It is fully compatible with the former optical links so that we can use old and new demodulators mixed without making any change in VME modulator. The same network communication schemes have also been ported to uClinux with almost full compatibility with the rpc source codes on VxWorks. The client application and APIs, therefore, can access the new boxes with a minimum modification for just increasing the numbers of clock/gate outputs. The cost advantage of the new unit is remarkably one-tenth the original VME one. It consumes only 1.2 W electric power, and thus will be a very reliable maintenance-free box without cooling fans. As such the semi-finished SoC platform is very useful to homemade an intelligent digitizer unit, another fast latching scaler (photon counting) module is now designed for LHD.

REFERENCES

[1] G. Raupp and H. Richter, IEEE Trans. on Nucl. Sci. **NS-39**, 198 (1992).

[2] H. Nakanishi, M. Kojima and S. Hidekuma, Fusion Eng. Design **43**, pp. 293–300 (1999).

[3] H. Nakanishi, M. Emoto, M. Kojima, M. Ohsuna, S. Komada and LABCOM group, Fusion Eng. Design **48**, pp. 135–142 (2000).

[4] J. Bloomer, *Power Programming with RPC* (O'Reilly, Sebastpol, 1991) [Japanese translation: ASCII, Tokyo (1995)].