DESIGN AND IMPLEMENTATION OF THE PULSED DIGITAL LLRF SYSTEM OF THE ESS-BILBAO ION SOURCE TEST STAND

H. Hassanzadegan*, N. Garmendia, ESS-Bilbao Consortium, Bilbao, Spain
F. J. Bermejo**, I. Del Campo, V. Etxebarria, University of the Basque Country, Leioa, Spain

Abstract

Design and implementation and some practical results of the pulsed digital LLRF system (amplitude, phase and tuning loops) of the RFQ for the ion source test stand in Zamudio-Spain are presented. The design is based on a fast analog front-end for RF-baseband conversion and a model-based Virtex-4 FPGA unit for signal processing and PI regulation. Complexity of the LLRF timing is significantly reduced and the LLRF requirements are fulfilled by utilizing the RF-baseband conversion method compared to the conventional RF-IF approach. Validity of the control loops is ensured practically by hardware-in-the-loop co-simulation of the system in MATLAB-Simulink using an aluminium mock-up cavity. It was shown through extensive tests that the LLRF system meets all the requirements including amplitude and phase stability, dynamic range, noise level and additionally provides a full amplitude and phase control range and a phase margin larger than 90 degrees for loop stability.

INTRODUCTION

The ion source test stand which is currently under construction in the Technology Park of the Basque country (Zamudio-Spain) will consist of a H- source, a front-end including a LEBT (Low Energy Beam Transport), an RFQ (Radio Frequency Quadrupole), a Diagnostic Vessel and a Beam Stop. The possibility of including a LINAC for energies up to 20 MeV is currently under study. The first stage of acceleration and beam focus after the ion source is the pulsed RFQ system driven by a klystron. The LLRF (Low Level Radio Frequency) system of the RFQ consists of an I/Q (Inphase/Quadrature) feedback loop to control the magnitude and phase of the pulse and a tuning loop to control the resonance frequency of the RFQ, hence minimize the reflected power with the presence of the beam. Table 1 shows a tentative list of the RFQ parameters (similar to the ISIS-UK RFQ system).

Based on these parameters a LLRF system was designed and developed by the ESS-Bilbao RF group in collaboration with the Electricity and Electronics Department of the UPV-EHU University and the ISIS laboratory to be used in the future for the RFQ system in Zamudio-Spain and also for ISIS front end test stand.

This paper is organized in three sections plus the final conclusions. The next section describes the three regulation loops (amplitude, phase and tuning). The following sections include the validation of the LLRF system by co-simulation as well as the test results.

* Corresponding author, email: hhassan@essbilbao.com
** F. J. Bermejo is also affiliated with CSIC
(Superior Advisor of Scientific Investigations)

Table 1: The RFQ Parameters

Parameter	Value	Unit
Nominal frequency	324	MHz
Amplitude stability	1	%
Phase stability	1	º
Tuning range	1	MHz
Unloaded Q	9000	
Peak RF power	1	MW
Peak RF voltage	3	MV
RF pulse width	250-2000	µs
Pulse repetition rate	50	Hz
Settling time (closed loop)	50-100	µs

IQ-BASED REGULATION OF THE RFQ

Amplitude and Phase Regulation Loops

Figure 3 shows a simplified schematic of the digital LLRF for amplitude and phase regulation. The design consists of an inhouse-developed analog front end, a digital unit with 8 ADCs and an add-on module with 8 DACs. The measured cavity voltage (from the pickup loop) is converted to baseband by an analog IQ demodulator board which is incorporated in the front-end unit. The I and Q signals, after some signal conditioning, are sampled by 14 bit ADCs running at 104 MSPS and fed into a Virtex-4 FPGA for the required signal manipulation including low-pass filtering, offset compensation, baseband phase shifting, feed-forward control and PI regulation. The I and Q outputs of the FPGA are then converted to analog by 14 bit 480 MSPS (4x interpolation) DACs and fed into the front-end unit where they are used as the baseband inputs of the IQ modulator generating the drive for the RF amplifier.

The magnitude and phase of the RFQ field during the pulse is controlled by setting proper values for the *Iref* and *Qref* inputs from the control computer (see Figure. 3). The use of the feed-forward signals (*IFF* and *QFF*) is two-folded. First, they can be used to operate the cavity in open-loop mode (In this case, the *OL/CL* switch is opened; therefore the IQ modulator is only driven by the *IFF* and *QFF* inputs). This mode can be particularly useful for test purposes or for making sure that the regulation loops will be stable before they are actually closed. Second, it can be used to compensate for repetitive or predictable errors (such as the beam) before these errors are sensed and corrected by the I/Q regulation loops.

The main advantage of the proposed control scheme compared to the conventional method (where the measured cavity voltage is first converted to an IF (Intermediate Frequency) by a mixer and then sampled at four times the IF) is that the complexity of the timing signals is significantly reduced. While with the conventional method several timing signals (f_{RF}, f_{RF}-f_{IF}, f_{IF}, 4*f_{IF}) need to be generated from the main RF source and the synchronization of these clocks must be ensured by a PLL (Phase-Locked-Loop) system, with the current design only f_{RF} and 2*f_{RF} would be needed for IQ modulation and demodulation respectively and that can be done easily using a frequency doubler.

Tuning Loop

The design of the tuning loop is also based on IQ demodulation. In this case, two IQ demodulators are used to convert the cavity forward and probe voltages to baseband and the resultant I/Q signals are sampled and fed into the FPGA. In the next stage, the phase difference between these RF signals is estimated by a phase discriminator which is programmed in the FPGA. Then, the tuning loop tends to keep this phase difference as close as possible to its desired value where the desired phase is the one giving zero reflected power from the cavity with the presence of the beam. This is done by defining two phase thresholds (typically ±2º) above and below the desired phase and keeping the actual phase always between these thresholds by moving the tuner inwards/outwards if the phase error exceeds either of the thresholds.

In order to prevent the tuner from moving continuously inwards and outwards (that can result an early wear out of the tuner hardware) the tuning loop is only activated during the pulse after the cavity field has settled.

LLRF HIL CO-SIMULATION

In order to minimize the time and effort for the establishment of the LLRF test bench, it was decided to co-simulate the FPGA hardware in the MATLAB-Simulink environment. With this method, known as HIL (Hardware-In-the-Loop) co-simulation, the FPGA communicates directly with Simulink blocks; therefore the FPGA hardware can be tested without having to connect it to the real-world signals. Then, Simulink source blocks were used to set the LLRF input parameters (such as the PI gains and the offset values) eliminating the need for an additional GUI (Graphical User Interface) and a communication protocol, while the I/Q input and output signals were still the real ones coming from the front-end unit connected to a mockup cavity. It should be noted, however, that although the HIL co-simulation of the loop proved to be very useful during the system development, test and trouble-shooting, for the final deployment it is foreseen to integrate the LLRF into the EPICS control system of the whole accelerator facility.

The control algorithms were developed on the FPGA using the Model Based approach [1] (instead of VHDL programming) as that also significantly shortened the development time and reduced the number of bugs in the FPGA algorithms.

PRACTICAL RESULTS

The LLRF system was low-power tested at the RF laboratory of the Electricity and Electronics Department of the UPV-EHU University with an aluminium mock-up cavity as shown in Figure 1.

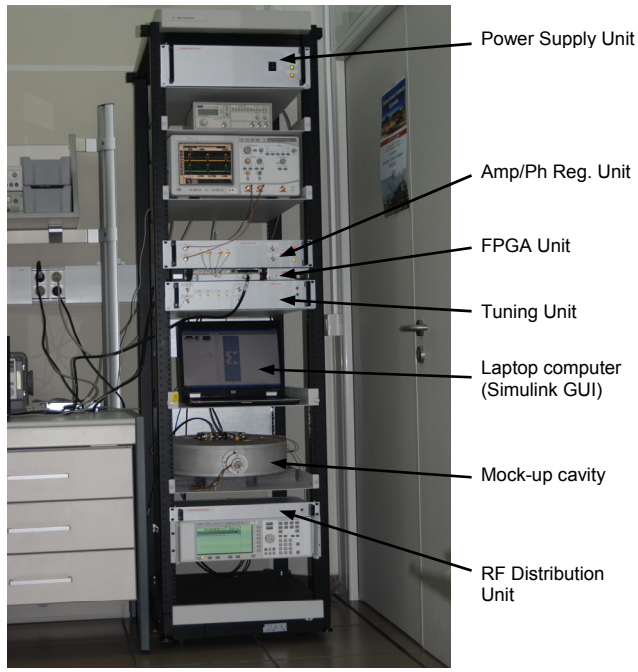

Figure 1: Picture of the LLRF test setup.

Table 2 shows the main parameters of the mock-up cavity:

Table 2: Main Parameters of the Mock-Up Cavity

Parameter	Value	Unit
Nominal frequency	327	MHz
Tuning range	1	MHz
Unloaded Q	1400	
Insersion loss	15	dB

While the regulation loops were regulating the cavity, the magnitude of the field was changed from zero to the maximum available from the RF amplifier and the phase was changed from 0º to 360º without any saturation or instability in the LLRF signals. In order to evaluate the performance of the regulation loops, a step-wise disturbance was imposed on the I/Q signals using the feed-forward inputs. The loops then removed the disturbance in 2 µs approximately. The total loop delay was measured at 800 ns approximately. From that amount, 500 ns was due the ADCs and DACs, 200 ns due to the baseband LPFs (Low Pass Filters) in the FPGA and about 100 ns due to the control program and cable lengths. It was shown, however, that even without baseband LPFs the stability requirements (1º, and 1%) could be achieved. Higher stabilities would also be

possible by utilizing stronger LPFs at the expense of increasing the loop delay and/or using other control methods. With the PI gains properly adjusted, the phase margin (in control theory, phase margin is the maximum phase that can be added to the feedback loop while still maintaining the loop stable) was measured at 110º approximately (i.e. ±55º on both sides of the optimum phase of the baseband phase shifter) providing a very large stability margin for the regulation loops. Figure 2 shows the measured cavity pulsed field (50 Hz) and the rising edge of the pulse with a settling time of 2 µs approximately.

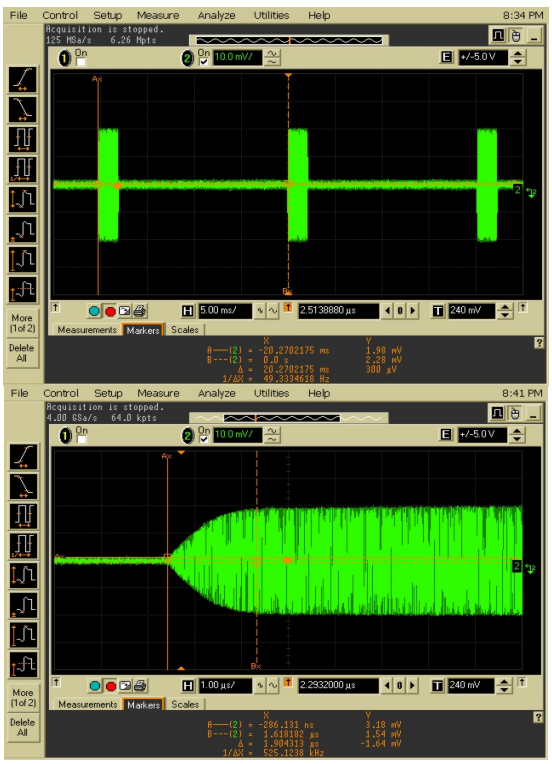

Figure 2: Measured cavity pulsed field (above) and an expanded view of the pulse at the rising edge (below)

Taking the quality factor of the RFQ and the bandwidth of the Klystron into account, the settling time of the pulse the final deployment is estimated at 30-50 µs which is well within the specifications.

SUMMARY AND CONCLUSION

A pulsed digital LLRF system was developed by the ESS-Bilbao RF group in collaboration with the Electricity and Electronics Department of the UPV-EHU University and the ISIS Laboratory to be used in the future for the RFQ system of the ion source test stand in Zamudio-Spain and also for the ISIS front end test stand. The LLRF system consists of an in-house developed analog front-end for IQ modulation and demodulation and a Virtex-4 FPGA unit for signal processing and control. The main advantage of the current design compared to the conventional method (i.e. based on RF-IF conversion) is that the complexity of the timing signals is significantly reduced. With model-based approach, the implementation of the system was eased and the number of bugs in the FPGA algorithms was reduced compared to the VHDL method. The LLRF hardware was co-simulated in MATLAB-Simulink using an aluminium mock-up cavity operated at low power. The results of these tests verified the ability of the LLRF system to meet all the LLRF requirements in addition to providing a fast response and a large phase margin for loop stability.

REFERENCES

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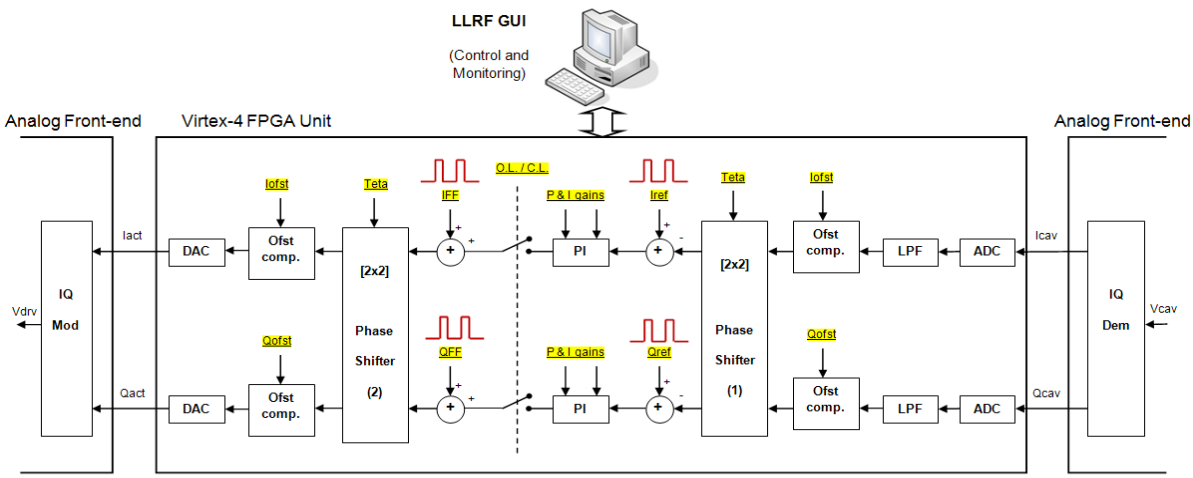

Figure 3: Simplified schematics of the FPGA program for amplitude and phase regulation; the parameters which are marked as underscore are set from the control computer.