NEW HARDWARE AND SOFTWARE DEVELOPMENTS FOR THE XFEL

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Abstract

The European XFEL is planned to be commissioned in 2014. This is time enough to consider modern and adequate technologies. After an evaluation phase, state of the art µTCA and ATCA hardware were selected as the core platform for the project. Ethernet and PCIe are the central communication links. Full remote management, hot-swap capabilities as well as a redundant architecture are further key features of this new standard. Java was selected as the programming language for the client applications. Two new DOOCS tools, written in Java, were created: the so called *jDTool* and *jddd*. *jDTool* is a generic data browser with spread sheet and plot capabilities. *jddd* is a full featured, easy to use display editor to create flexible control system user interfaces. Both tools can communicate directly with DOOCS, Tine, Tango and EPICS. The experience with the new hardware platform and the new applications will be discussed.

NEW HARDWARE DEVELOPMENTS

TTF started 1993 with design decisions [1]. In this period VME was a mature standard used by many institutes. Therefore it was a natural decision to use it for TTF. The XFEL is planned to start commissioning in 2014. Today VME is already 27 years old and it's time to reconsider the question of an adequate standard for this project. A workshop was held to address the question of selecting a crate standard for the European XFEL. It was agreed to use ATCA and µTCA (short xTCA) as the main platform. Before it came to this decision an intensive discussion took place to compare the alternatives. Two alternatives turned out to be the best candidates: VME as a well known system and xTCA as a new technology.

VME

As mentioned, VME is 27 years old and has some pros and cons:

- Number of new developments is decreasing, sales are still constant
- Bus technology has speed limitations
- Wide busses create a lot of electrical noise in analog channels
- No standard management on crate level
- No management on module level
- So far no extension bus survived
- One damaged bus line stops a whole crate
- Module exchange in a powered crate causes hardware and software damage
- Address and interrupt misconfigurations are hard to find
- A lot of I/O modules are available
- Good knowledge and long time experience is available

µTCA Features

The Micro Telecommunications Computing Architecture is the most recent standard in the field. It was initiated by the telecom industry. The main features are:

- Scaleable modern architecture: from 5 slot µTCA to a full mesh ATCA
- Based on Gbit serial communication links
- High speed and no single point of failure
- Standard PCIe, Ethernet and SRIO communication
- Redundant system option
- 99.999% availability is possible
- Well defined management: a must for large systems and for high availability
- Allows full managed hot-swap of modules: is safe against hardware damage and software crashes

Availability is defined by UpTime / (UpTime + DownTime). The downtime or the time it takes to detect a failure and to repair it has to be minimized. A good management helps to early detect failures and to diagnose problems. In a large system it is also important to manage the installed hardware and firmware. This management is well defined in xTCA and is implemented in all modules. The excellent management, the modern communication standards Ethernet and PCIe together with the hot-swap functionally are the key arguments for the selection of xTCA.

Results of the Crate Standards Evaluation for XFEL

Before the decision the new xTCA system was evaluated. To find incompatibilities and to prove the completeness of the standard crates, CPUs, IO-modules and the MCH (switch hub) were used from different vendors.

The results are:

- Management of crates is well implemented
- Dynamic module and crate info gives all relevant info
- Fast data transfers (>400MB/s on 4 lanes PCIe)
- Hot-swap works (tested with Solaris and Linux)
- PCIe and Ethernet drivers are part of operating systems
- Good electrical decoupling of modules on the backplane
- Good analog performance
- µTCA standard requires a few additions

The general conclusion is that the xTCA platform is a good basis for large installations. Since the specs are made for telecom industry, a few things are missing for the applications in the accelerator field: clocks, triggers and interlock signal distribution as well as more space for

IO and signal conditioning. To add these features a working group at the PICMG standardization was initiated. This group is called “xTCA for Physics” and includes accelerator institutes and xTCA vendors.

PICMG Activities

The hardware working Group has the goal to define in 2009:

- µTCA rear transition modules – rear I/O for AMC
- Additional connector / selection of existing pins
- Rear I/O on ATCA carriers
- Define pins for I/O on backplane
- Clock and trigger distribution (ATCA and µTCA)
- Allow data Acquisition with ps stability
- Guidelines for timing and synchronization
- Define recommended AMC board sizes
- Specifications for ATCA RTM

To verify the proposed standard a double size ADC development with 10 channels and 16 bit resolution with a speed of 125 MSPS has been initiated. Different

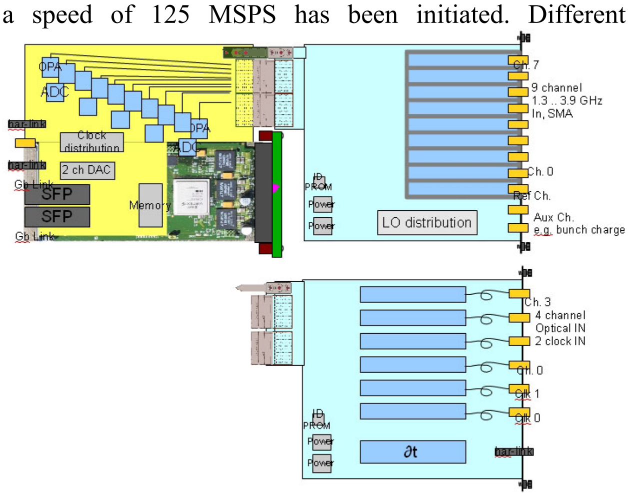

Figure 1: Proposal of a double size AMC module (left) with two different Rear Transition Modules (right).

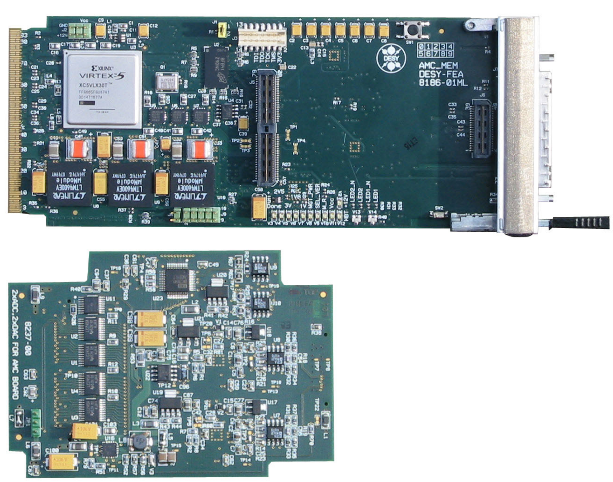

Figure 2: DESY development: AMC with FPGA and piggyback equipped with 2 channels of ADC and DAC with 125 MSPS each.

measurement application interfaces can be implemented on Rear Transition Modules (RTM). These double size modules provide more space for electronics than on a VME board.

A second working group for software was also setup to find ways of standardization in the communication between various parts of the system. The goal is to provide guidelines and shareable code. It is planed to have results in 2010.

Hardware Developments

As part of the evaluation process a universal AMC board with a Virtex 5 FPGA was developed at DESY (Figure 2). The board has a plug for a piggyback module. A module with two ADC and two DAC channels running up to 125 MSPS was designed to check the analog performance. The PCIe readout with 4 lanes is implemented in a Virtex 5 FPGA.

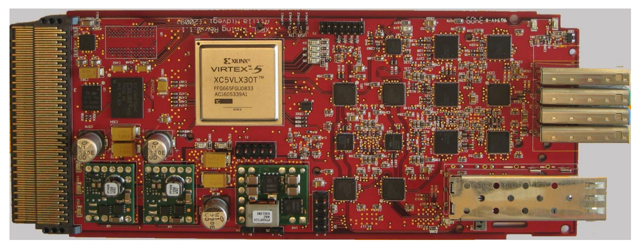

Figure 3: University of Stockholm development: Timing system AMC board.

Furthermore a Timing AMC is in development (Figure 3). This design is done by the collaboration partner from the University of Stockholm. The developed module contains both, the transmitter and receiver part. Timing and clock information are transmitted by a coded 1.3GHz data and clock train. A synchronization and drift compensation schema should provide a ps stable clock at any distributed receiver along the 3.5km long linac.

Crate Management

After the successful design of hardware the management of the xTCA had to be verified. The management is defined on basis of IPMI for all parts of the system. To be able to read for instance the temperatures of a certain module and to compare it with a drift measurement of an ADC it was necessary to integrate the management system into the common DOOCS control system. Figure 4 shows the management architecture. ATCA and µTCA crates are connected via IPMI over Ethernet to a central DOOCS server. The server reads all information of the crates and actually installed modules via IPMI commands. With this information it generates dynamic addresses and properties according to the detected hardware. The IP address of a crate is the only required configuration parameter to be supplied to the server. The newly developed applications *jddd* and *jDTool* are used to display data to the user.

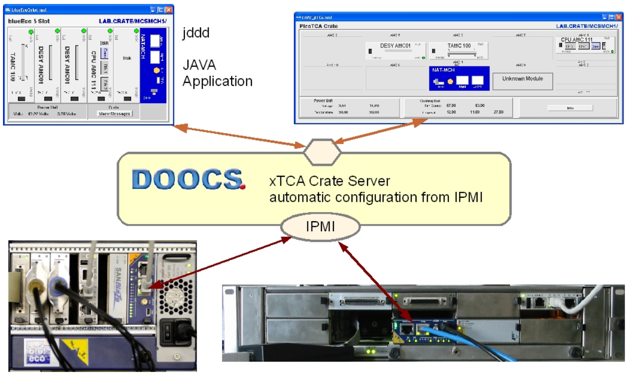

Figure 4: Crate management architecture.

NEW SOFTWARE DEVELOPMENTS

A Java based editor and display manager was developed as a GUI environment. It allows subsystem experts to develop their own panels without knowledge of a programming language. A second generic new tool is the so called *jDTool*. It provides access to all control system values.

jddd

With the help of a rich set of widgets, including animated graphics and plots the user can easily design very complex control system panels (Figure 5). The created designs are hierarchical. Such a hierarchy can include other drawings as components. Furthermore it provides a plug-in interface to integrate foreign widget sets [3].

jddd is build on top of the jdoocs library to support 4 different control systems: DOOCS, TINE, Tango and EPICS. The access is fully transparent to the user since it is handled by a DOOCS name server. Furthermore an address of a variable or channel can contain the control system name to directly talk the native protocol without referring to a name server. Further details are available on a Web site [4].

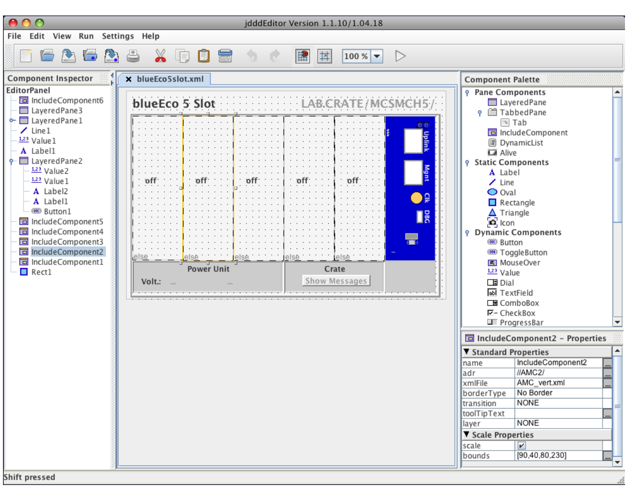

Figure 5: The *jddd* editor.

jDTool

This Java based DOOCS Tool shows all available addresses of the control systems in a tree view. The tree is dynamically generated from the data of a name server and the actual parameters from device servers. The four different views present the data either in a spreadsheet, as lists, in plots or in a text editor with XML capabilities (Figure 6).

jDTool can be used as a Save&Restore tool too. It saves selected data as well as chosen selections in files.

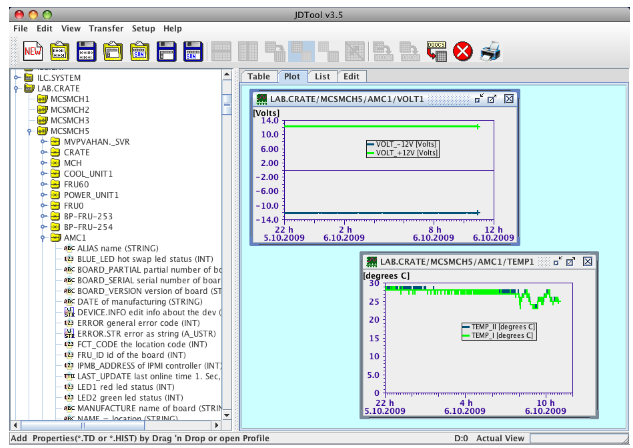

Figure 6: *jDTool* shows the voltage and temperature histories of an AMC module.

CONCLUSIONS

The XFEL will be based on the state-of-the-art xTCA hardware platform. Tests have shown that this standard is a good choice and it's worth the effort of conversion from the old VME system. A full integration of the hardware management into the DOOCS control system was also demonstrated. This allows using the new developed display tools to show dynamically the hardware status and other relevant information.

The results and products described in this paper were developed by the FLASH and XFEL controls group and the collaboration partner of the University of Stockholm.

REFERENCES

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