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Beam Position Monitor Multiplexer Controller Upgrade at the LAMPF Proton Storage Ring*

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Abstract

The beam position monitor (BPM) is one of the primary diagnostic tools used for the tuning of the proton storage ring (PSR) at the Clinton P. Anderson Meson Physics Facility (LAMPF). A replacement for the existing, monolithic, wire-wrapped microprocessor-based BPM multiplexer controller has been built. The controller has been redesigned as a modular system retaining the same functionality of the original system built in 1981. Individual printed circuit cards are used for each controller function to insure greater maintainability and ease of keeping a spare parts inventory. Programmable logic device technology has substantially reduced the component count of the new controller. Diagnostic software was written to support the development of the upgraded controller. The new software actually uncovered some flaws in the original CAMAC interface.

I INTRODUCTION

The Beam Position Monitor (BPM) system is the primary tool available for beam tuning at the Clinton P. Anderson Meson Physics Facility (LAMPF) Proton Storage Ring (PSR). The BPM multiplexer controller is an integral part of the BPM system. The multiplexer controller is the interface between the BPM[1] system hardware and the PSR microVAX data acquisition and control system, see Figure 1. There are approximately seventy BPM's that are used as a primary tuning tool by PSR operators.

The existing multiplexer controller was difficult to troubleshoot and repair. The old controller was built on 12 wire-wrap "CASH" cards mounted in a 19 inch rack mount chassis. A spare controller chassis was never built, making on line troubleshooting to the component level necessary.

The analog to digital converters that were used in the original design are no longer available. It should be noted that conversion must occur with in the time constant of the circulating proton bunch in the ring, 360 ns.

In addition, there were no software diagnostic tools to aid in troubleshooting and testing.

Several factors affected design of the new controller. Programmer resources were not available to write code for a more modern microprocessor so we needed to do an Intel 8085-based design and reuse as much of the 3000 lines of original assembly code as possible. The new controller needed to be modular so that "card swapping" could be used as a troubleshooting and repair technique. We wanted to use as many off the shelf components as possible. The new controller needed to be as "plug compatible" with the old controller as possible, so that no modifications to other components of the multiplexer system were necessary.

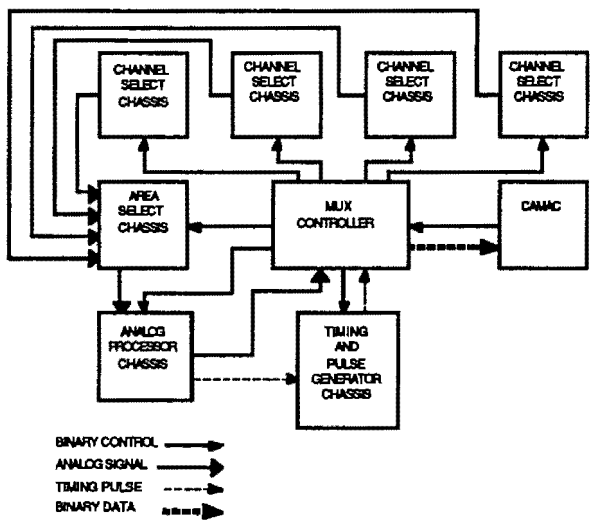

Figure 1. BPM System Block Diagram

We elected to do the project in a STD bus format. STD bus is a mature, well defined, well supported industry standard. The STD bus standard was designed for 8-bit microprocessor control functions, and several vendors offer 8085 CPU cards. In addition, several vendors offer well-built chassis with terminated back planes.

II. CONTROLLER FUNCTIONS

When the BPM control software running on PSR microVAX needs data, it sends a command/request list via CAMAC, to the controller. The request defines which channels are to be read, number of samples per channel, and timing information. The command list is loaded into a CAMAC output FIFO(First In First Out buffer) and then signals the multiplexer controller, via a CAMAC TTL output module, that the FIFO is loaded and ready to be read. The controller reads the FIFO, stores all the command/request information in RAM.

The controller takes a number of actions prior to actual data acquisition. It must first select the channel and area multiplexer that corresponds to the BPM whose position information has been requested. The controller writes to a timing chassis to set up trigger and timing parameters and it writes to the analog signal processor chassis to set gain and

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attenuation of the BPM front-end analog processor. Finally, its internal counters are initialized to begin counting channels and samples per channel. After the set up is complete the controller accepts analog signals and begins analog to digital conversion.

When the controller has acquired all the requested beam position information, it formats the data, flags any known bad data, and loads it into a CAMAC input FIFO. Then the controller pulses a CAMAC input register that sets an interrupt for reading the BPM data that has been loaded into the input FIFO.

III. CIRCUIT DESCRIPTION

A. CAMAC Interface Circuit Board

The CAMAC interface card is the interface between the controller and the CAMAC crate connected to the PSR microVAX via a CAMAC serial highway.

B. I/O Functions Circuit Board

The controller talks to the Area Select chassis, the several Channel Select chassis, and the Timing and Gate Generator chassis via the three I/0 cards. All three cards are similar in that each card decodes I/0 write instructions and latches the data bus into buffers. The differences are that the port addresses differ from card to card.

The instruction decoding, on all the I/0 cards, occurs in programmable logic device (PLD) decode chip.

C. Timing and Control Circuit Board

The Timing and Control card generates the timing pulses that other cards use to initiate analog to digital conversions, strobe data in to RAM and increment counters.

D. Analog to Digital Conversion Circuit Board

The three A/D cards, one each for horizontal position, vertical position and beam intensity are identical except for the address decoding jumpers.

F. Beam Status Module & Counter Module

The Beam Status card uses one bit of a 2K RAM to store whether or not beam was present at the time of an analog to digital conversions.

The microprocessor subroutine that packs the data for shipping to the VAX looks at the beam status data and flags the horizontal and vertical position data if beam was not present. The bad data flag is an 80h[2] in the position byte. When the VAX software sees the 80h in a stream of data it ignores that byte and does not attempt to display it.

The main function of the counter card is to count Samples Per Channel (SPC).

G. CPU Circuit Board

The CPU is a commercial STD board available from Microlink, a division of Sea-Ilan, Inc.[3] .

We have made several changes to the CPU card to accommodate non-standard STD Bus signals that are routed on the STD backplane.

The 8085 is designed to boot to address 0000h however the ROM on the CPU circuit board resides at 2000h. We have included a special boot sequence to take care of this.

H. Chassis/Backplane Circuit Board

The multiplexer controller resides in a Matrix Corporation "Blackplane" STD bus card cage. The chassis was purchased assembled with back plane and fused and switched power supply. The power supply is rated at 5 volts, 25 amps and +/- 12 volts, 3 amps.

IV. SOFTWARE

Of the 3000 lines of 8085 assembly code that is the heart of the controller, only about 20 lines needed to be changed. Most of the changes were in response to the hardware-specific boot sequence required by the new CPU card. The mapping of memory needed to be modified in order to accommodate the address space available on the commercial STD cards.

A PC-based (MS-DOS) diagnostic was written to assist in the development of the new controller. The program was written in C with a modifications to the software library supplied with the CAMAC crate controller used for our CAMAC-multiplexer testbed so that software interface to the library routines was the same as those on the PSR microVAX. The source code for the diagnostic program was easily ported to the VAX with very few changes.

The VAX-based diagnostic can be run from any VT-type terminal. One can modify the command list which is sent to the multiplexer controller. By modifying the command list one can control channel selection, time into pulse, time into cycle, trigger selection, sensitivity, and samples per channel. The diagnostics will send the list to the controller, handling all the handshaking just as the production software used by the operators does. When the controller has acquired the data it saved to disk,where it is available for viewing and analysis.

The diagnostic program uncovered a CAMAC interface timing problem, that existed with the old controller, which had the potential to cause data to be lost.

V. RUN-TIME EXPERIENCE

The controller has been used for about four months of PSR production. We have had no major problems with the system. The addition of needed diagnostic software has allowed us to accurately pinpoint the sources of problems that have come up.

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[1] E.F. Higgins and F.D. Wells, " A Beam Position Monitor System for the Proton Storage Ring and LAMPF", Particle Accelerator Conference, Washington, DC USA (1981)

[2]The lower-case "h" indicates a hexidecimal number.

[3] "STD-245, 8085A Single Board Computer, Operations Manual" Microlink, a division of Sea-Ilan, Inc.,14602 N. US Hwy 31, Carmel, IN USA 46032