ISBN: 978-3-95450-254-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS1991-S09DPP03

Intelligent Trigger by Massively Parallel Processors for High Energy Physics Experiments

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Abstract

The CERN-MPPC collaboration concentrates its effort on the development of machines based on massive parallelism with thousands of integrated processing elements, arranged in a string. Seven applications are under detailed studies within the collaboration: three for LHC, one for SSC, two for fixed target high energy physics at CERN and one for HDTV. Preliminary results are presented. They show that the objectives should be reached with the use of the ASP architecture.

I. Introduction

High luminosity hadronic colliders (LHC & SSC) will require novel detectors, both highly time-sensitive and selective. Potentially, Megabytes data will be produced at rates (66 MHz at LHC) that are beyond performance of today modern transmission and recording technology. From this huge amount of information, however, only a tiny fraction is possessing any real interest. The required high selectivity is assumed to be achieved by a two steps procedure. A first-level decision based on simple "hard-wired" logics can provide significant rate reduction, it leaves, however, for the second-level decision so complex patterns which require a detailed analysis similar to what is done today in off-line programmes, but with an event frequency of typically 100 kHz. Such decisions, based on a huge number (10 to 100 Mbytes) of digitised local or global data coming in a narrow time window, will require the fast execution of precisely tuned algorithms in extremely fast computer-like devices. Industry and computer science make serious efforts in this field. The MPPC (Massively Parallel Processing Collaboration) is concentrated on problems that are likely to benefit from massive parallelism of SIMD type. Such massively parallel machines operate with thousands of processing elements, all highly integrated and controlled under a single controller. Taking advantage of the application needs and of the coincidence between technological opportunities - the development of a new kind of SIMD machine by ASPEX Microsystems (UK): the ASP (Associative String Processor [1]) and the continuous improvement in silicon integration (VLSI/WSI) - a Research and Development programme "The MPPC Project" has been launched [2-5] between ASPEX (UK), CERN (CH), CEA/CEN-Saclay and CNRS/IN2P3-LAL-Orsay (F), as main partners, and EPFL-Lausanne (CH), University of Brunel (UK), University of Geneva (CH), CRIP/KFKI Budapest (H) and Thomson-TMS (F), as associated partners. The applications are dominated by but not exclusively driven by the problem of triggering events in HEP; EPFL, as MPPC partner, is indeed working on a first application in image processing for HDTV. More generally, it can be expected that the same basic processing elements will find their way into quite different application fields. Indeed, the almost infinite scalability of the ASP architecture[1] and its impressive performance targets (in terms of cost, power and achieved density) will attract other suitably parallelized projects (e.g. relational data processing, simulation, computer vision, cellular automata, neural networks) in applications such as, high-definition TV, autonomous guiding vehicles, artificial intelligence, medicine, space science, meteorology, plasma physics, etc. Even one can think about possible application for on-line accelerator control.

II. The ASP architecture

The choice of the ASP, as a R & D platform for the Collaboration, was based on the exceptional potentialities offered by this new architecture which allows a wide range of applications.

The main hardware task is to build four ASP machines, one for each main partner, with 16384 APE array, referred to as the "MPPC array". It is based on the existing VASP-64 VLSI ASP chip used for the TRAX-1 machine, another ASP project dedicated for off-line image processing [6,7]. The MPPC-array design allows for maximum processor element density and maximum direct parallel interfacing via conventional electronics to the readout of particle detectors. For this task, dense packages of ASP must be constructed. This is based on a modular design, using hybridation on insulators of the VASP-64 chips. These modules are built by PolyCon (USA) ; they contain a string of 1024 APEs (16 chips) with two parallel I/O per module. These modules will be installed on boards to make 8K strings. Two ASP boards and a low level controller (LAC) in extended VME standard (in order to be compatible with existing industrial modules) are under construction for each 16-K MPPC-Array machine.

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A. *Associativity and string features*

The ASP consists of associative processing elements (APE) working as SIMD machines. The string can be arranged in a loop: the architecture is reconfigurable by programmation. Each APE is an associative memory cell with processing capability. Synchronous and asynchronous communication between APEs is provided through an inter-APE communications network dynamically reconfigurable. APEs are addressed by content through a common bus, which minimises data movement. Parallel processing is performed on active APEs selected at a given step of the programme. The architecture is scalable up to hundred of thousands APEs, due to high integration (VLSI/WSI) and low power consumption (~ mW/APE). The low target cost (below 5.- SFr per APE) is leading, together with the low power and high integration capability, to the possibility of massive integration. The system has maximum application flexibility and computational efficiency. It is fault tolerant: blocks of faulty APEs may be disactivated without breaking the string . The MPPC-Array machines will have Parallel I/O capabilities (10 Gbit/s). ASP application programmes can be written in any block-structured language (Modula 2 is the commonly used language). An introductory course to ASP, provided by ASPEX, is useful to reach a good level on the learning curve in parallel algorithms.

B. *ASP chip and module*

The basic chip for the construction of the compact hybrid MPPC modules (HASP) consists of a programmable VLSI SIMD parallel processing device, incorporating 64 associative processing elements (APE, see fig.1 and 2): the Aspex Microsystems Limited VASP VLSI ASP chip presently manufactured with 2μm technology at ES2 (F).

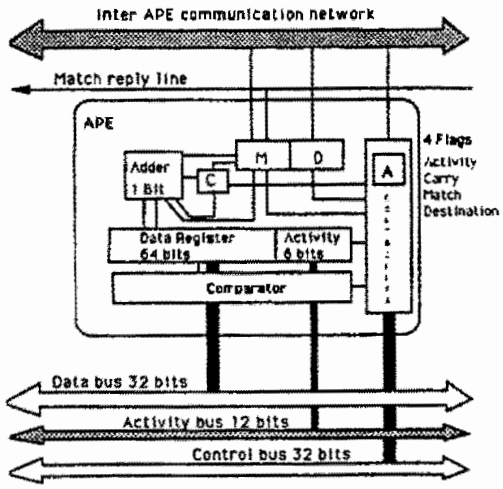

Fig. 1 - Schematic of the associative processing element

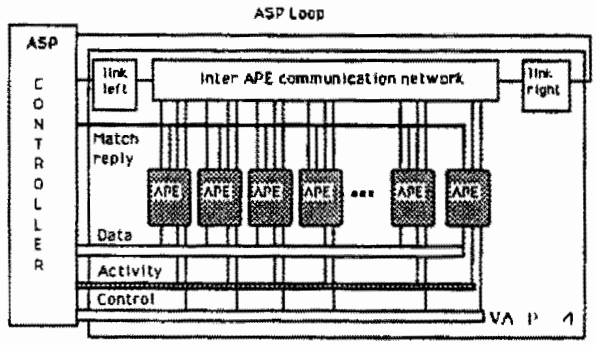

Fig. 2 - The basic Associative String Processor

This chip, although slower than expected, is suitable for making the first prototype hybrid HASP module . This module is under development at ASPEX for the MPPC-Arrays and is to be manufactured by the sub-contractor Polycon Inc. (USA). For second-level triggering experiments a faster device will be required. It will use a 1.2μm SOS (silicon-on-sapphire) device in order to achieve a fully working 25ns VASP chip in the summer of 1991 (a high performance ASP chip presently developed by ASPEX and Hughes Company). It will be the basic stone for the final hybrid ASP module for MPPC-arrays: the HASP/P1. This 1K APE module, using 16 dice, has a bypass of 64 and 256 APE blocks and 2 I/O ports which can be configured as 2 x 512 APE substrings or a 1K substring with a LAC interface and an ADB (ASP data buffer) interface. The design is targeted to a standard 184 pin package (3" x 3" with leads).

The operating system and programming tools are ready for a test using the controller (LAC prototype) under construction at Saclay.

C. *Machine architecture*

Each MPPC-Array will be composed by one LAC and two ASP boards giving a 16 K machine. In concentrating all ASP boards in the same machine we will have the 12-bit addition). The ASP board will use the hybrid modules. Each ASP board will contain 8 modules giving a number of 8192 APE per board. Each module will have its own data exchange and ADB double port memory to allow a faster feed for data

III. Applications: Status and First Results

As previously stated, seven applications are studied: three LHC oriented, one SSC oriented, two for fixed target

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physics at CERN and one for HDTV.

A. *Muon selection at LHC (CERN)*

At LHC single and multi-muon triggers will play a crucial role in particular for Higgs search through its four leptons decay. An analog first-level muon trigger is expected to cut down the single particle rate below 10^5 Hz. In order to identify the muons, a more sophisticated second-level trigger is further required. This includes momentum determination, charge assignment and counting all the tracks which are above a given cutoff momentum. This task must be achieved in less than $\sim 20\mu s$ in order to cope with the rate of the first-level trigger. The solution which is under study proposes to divide the triggering procedure into three phases: the loading of the hit information coming from the muon detector (detector mapping into the ASP), the preprocessing of the data (determination of the best hit positions: the "Master point determination") and the tracking (track finding, charge signature and p_T determination).

Taking advantage of the rotational symmetry of the CMS detector model [8], a (r, ϕ) mapping of the fine-grain muon detector can efficiently be done in the ASP [9]. A track is defined in the central plane of projection (plane of deflection perpendicular to the beam axis) by the vertex of the interaction, positioned with high precision, and by the muon trajectory detected at five radii with multilayer detectors . The mapping is done in a way which associates one APE to each $\Delta\phi$: this allow to identify in a single search all the high p_T tracks. The granularity $\Delta\phi$ (typically in the mrad range) is a parameter dictated by the size of the Coulomb-scattering. As long as $\Delta\phi$ is above its minimum physical detector pitch value, the mapping is reconfigurable according to the chosen triggering p_T threshold.

Only the active cells are loaded into the ASP, preserving the topology of the detector which provides the so-called "iconic mapping". Then, a "master-point" is calculated from the multi-layer detector hits, taking into account detector inefficiency and possible multiple hits in one or more layers. This preprocessing is done using a fast "iconic average" using data shifting and bit-logic operations across the APEs. For the third step of the triggering scheme, the tracking, iconic algorithms use bit representation of the image of tracks and the image processing can be done bit parallel in the ASP machine. The five consecutive values of the azimuthal angle ϕ relative to the innermost ϕ_0 value, expressed in unit of $\Delta\phi$ is used for calculating a "track-code ". The track-code is a unique representation of a given charged particle trajectory through the muon detector. A preliminary study was to construct track codes from the Geant Monte Carlo data and to explore the feasibility and efficiency of triggering by the proposed iconic algorithm. It consists of looking for all hits at the same time for a fit between master points configuration and all possibilities of track-codes. The number of track-codes depends on the ϕ binning. This number determines the muon search execution time. On the contrary, the triggering time will not depend upon the muon multiplicity because the search is done in parallel over all ϕ_0 and ϕ values. For triggering purpose ($p_T \geq p_T$ threshold) a momentum is determined for each track, by assigning to each track-code a maximum p_T value using a simple look-up table. The preliminary results of the simulation show that the trigger can be worked out within about 20 μs: 5 μs for loading, 5 μs for preprocessing and 10 μs for tracking. This timing fits the requirements imposed by the expected first level trigger rate at LHC.

B. *TRD electron selection at LHC (CERN)*

An integrated transition radiation detector (TRD) and charged particle tracker has been proposed for a LHC detector in order to improve the identification of electrons beyond the level of electromagnetic calorimetry[10]. The TRD tracker will have about 500 000 channels (straws) put inside a cylinder installed around the beam axis (the Halo model). Electron candidates will be tagged by a surrounding calorimeter and the information will be used to define planes cutting the tracker detector and defining candidate roads inside the TRD. One assumes limits on both, the number of candidates (no more than four per event) and the rate of candidate occurrence (not more frequently than every 10 μs average). The basis of discriminating electrons from hadrons in the TRD tracker lies in the statistical analysis of pulse heights of all digitising belonging to a track candidate. This allows to measure the probability of TRD X-ray emission (and detection), which is strongly enhanced for electrons due to their very high γ values. As for the muons, the trigger procedure can also be divided into three phases, but each of them is being implemented on a different type of hardware for optimising the running of the dedicated algorithms.

C. *LHC calorimetry, jets and shower detection (Orsay)*

The use of ASP at the second-level trigger of a barrel calorimeter model for LHC is under detailed study using the ASP simulator. It is assumed that the event buffering at that level should not exceed 100 μs on average. Special care is put on the study of the mapping of the calorimeter cells into the ASP (patching optimisation). The basic procedure is to associate one APE to each cell. The loading time will be of the order of 10 to 15 μs. If the Vector Data Buffer feature (VDB: a word parallel, bit serial ASP loading under development at ASPEX) becomes available on the chip, most of this time will be overlapped with the processing of the previous event, and the real cost of loading will only be 1 μs. A fast rejection of each event detected inside the calorimeter should be done in an aver-

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age time of 50 μs. Jet energy, isolated electrons, missing energy, shower shape and position are the essential event feature extracted from the calorimetry. Various selection algorithms are under detailed study. They are based on the analysis of the energy deposited in neighbouring cells, making correlations between the information coming from the electromagnetic and hadronic parts of the calorimeter. The possible use of preshower detector is also considered. As a result, 20 to 30 μs processing time is obtained.

D. *Possible use of ASP for SSC/SDC detector (Saclay)*

At SSC, the measurement of jet energies is essential for the detection of neutrinos and others unseen particles. The SDC (Solenoidal Detector Collaboration) detector [11] is based on a (ϕ, η) tower segmentation where ϕ is the azimuth angle and η the pseudo-rapidity ($\eta = -\ln\tan\Theta/2$ where Θ is the polar angle). Each tower is logically divided into five layers providing the symbolic information which will give the necesary event topology and e/h/μ particle identification used for triggering. Starting from the vertex, the five layers of detectors give the following information: tracking (hits/track), answer for isolated electron, number of electron clusters, number of hadron jets and muon hits. In the calorimeter, an isolated electron pixel is characterised by an electromagnetic energy value greater than an e.m.-threshold, a hadronic energy value lower than a hadronic-threshold, and no direct neighbouring cell with e.m.-energy greater than an other e.m.-threshold. The basic principle of using ASP in a second-level trigger is to associate one APE for each calorimeter cell and to load into this APE all the information about the five layers contained within a corresponding (ϕ, η) tower. Inside each APE, the 64 bit data register is enough for storing all this information. For the detection of missing energy, the calculation of the transverse energy E_t is done by summing $E_{sin\Theta}$, calculated simultaneously in the APEs for each cell. Preliminary results of algorithms simulation using the VASP-Simulator give 7 μs for the detection of isolated electrons and $\sim$ 20 μs average time for missing energy (dependent on clusters number and geometry).

E. *A K_0 trigger for NA48, a fixed target physics experiment at CERN (Saclay)*

The NA48 experiment is an experiment aiming to perform, in 1994-96, a high precision measurement of the ϵ'/ϵ parameter in order to have a better understanding of CP violation [12]. This parameter is determined from the measurement of charged ($\pi^+\pi^-$) and neutral ($2\pi^0$) decays of K_0^S or K_0^L, concurrently. The target is to obtain on-line a very good signature of $2\pi^0$ candidates in less than 10 μs, taking as inputs the energy deposits in the 12000 cells of an electromagnetic calorimeter array. Candidates should give exactly four photon shower clusters in the detector. Physics constraints from the K_0 decay are used for validating good triggers: the transverse momentum conservation implies zero value for the first moment of the energy distribution (relative to the centre of the calorimeter) and, from the K_0 mass constraint, the vertex position can be calculated by using second moment of the energy distribution and total energy of the clusters. These calculations should be invalidated if an accidental hit occurred in the calorimeter in the sensitive time window. Processing time was evaluated for the ASP and for digital signal processors (DSPs). ASP is better suited for the topological processing tasks (find clusters and count them, find accidentals and locate them relative to the normal signal timing), while DSPs are better on the fast, high accuracy, stream arithmetics required in the energy balance and vertex calculations. This application is an example of the use of ASPs in prompt trigger systems, where real time response performance, and fast parallel loading capability is of prime importance. The result of this study shows that combining ASP and DSP processors in the fast neutral NA48 trigger system is currently sufficient to fulfil the NA48 requirements: an efficient $2\pi^0$ trigger can be performed in less than 10 μs.

F. *ASP tracking with CCD on-line camera in WA93, a fixed target heavy ios physics experiment at CERN (U. of GENEVA)*

A heavy ion experiment (WA93) is scheduled at CERN with the aim to study Bose-Einstein correlations among charged pions. The reconstruction of the pion momenta with a large acceptance will be done with a tracking system consisting of a spectrometer magnet and new type of light emitting multistep avalanche chambers[13]. The passage of a charged particle through the chamber is detected as a cluster of light registered by Megapixel CCD cameras. The analysis implies various stages: image preprocessing (back ground reduction and subtraction, optical distortions) then actual image processing (cluster analysis) and finally tracking and momenta correlation . The use of ASP for these tasks looks very promising as they are well adapted for massively parallel image processing. Bose-Einstein correlation requires computation of four-momentum difference for all pairs of tracks which means that many TFLOPS of computing power will be required for only a few days of running ($\sim 10^6$ events).

G. *Image sequence coding, data compaction for HDTV (EPFL)*

At the signal processing laboratory (LTS) in EPFL, the image sequence coding group has developed number of techniques for image sequence compression reaching very high compression ratios. For real time processing at video rate of large images, a parallel computation approach is necessary. This is why the use of ASPs is studied using two different methods: the parallel implementation of the

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Gabor compression algorithm [14] and the parallel implementation of artificial neural networks on the ASP [15]. In the Gabor compression algorithm, the image is decomposed in elementary Gabor functions basis. The use of such a decomposition is motivated by the fact that Gabor functions have optimal localisation in both spatial and frequency domains. The realisation of this algorithm requires the study of efficient parallel algorithms for matrix computation, particularly large matrix multiplication (typically 256x256). Several algorithms for matrix multiplication on ASP are under study. At this time, two programmes for integer computation have been developed, one using 8 bits and one 16 bits. The best results have been obtained with an algorithm called outer product [14]. The initial results obtained with the ASP simulator in function of the matrix dimension for 8 and 16 bits integers are very encouraging in view of video rate compression up to 200:1 ratio.

IV. Conclusion

From the applications under detailed studies for high energy physics at the future hadron colliders LHC, SSC and for SPS fixed target experiments at CERN, preliminary results obtained from simulations, based on the use of ASP machines developed in the MPPC project, can be summarised as follows:

- a second level muon trigger at LHC is feasible and could be done within about 20 μs.
- a second level trigger for calorimetry at SSC and at LHC would require something like 50 μs,
- for the NA48 fixed target experiment, a $K^0 \rightarrow 2\pi^0$ trigger could be achieved in less than 10 μs.

All these results are encouraging and could fulfil the ambitious objectives of these applications. In another domain, for HDTV and videophone applications, preliminary results for compression and restoration of images show that using ASPs could open the possibility of working algorithms at video rates. Real time tests for the seven applications studied at present should be possible in about a year, when the four MPPC-array machines become available.

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