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CONTROL SYSTEM OF THE SILICON MICROSTRIP LAYER FOR THE STAR EXPERIMENT.

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The Silicon Vertex Tracker (SVT) in the STAR experiment at RHIC makes use, in its outer layer, of silicon-strip detectors. This layer is a barrel of 320 double-sided detectors. The 768 strips of each detector's side are read out by 6 ALICE-128C analog front end chips. Those chips are remotely controlled, using a JTAG protocol. Another chip, the COSTAR, has been designed to perform "in situ" front end measurements (temperature, low and high voltage supplies, detector's bias currents). It uses the same JTAG protocol and is implemented on the same bus. The use of this bus provides a high granularity (each parameter drives a set of typically 768 or 128 channels out of about 500000). The control system can be divided in two parts. The first is the "slow control" which main purpose is to monitor and control the "slow" parameters (temperature, power supplies, etc.). The second part is the detector control which has to control the front end to calibrate the detector and to provide a current status of the SSD layer. The Operator Interface is a Sun workstation, running EPICS. The Input Output Controller is a VME crate. The LAN is Ethernet, using the TCP/IP protocol.