A PROTOTYPE ATM NETWORK FOR LHC BEAM CONTROL

T. Wijnands, CERN; W. Herr, CERN; P. Ribeiro, CERN

ATM is a candidate technology for the site-wide communication of timecritical machine data of the LHC. In this paper, first results of aprototype ATM (Asynchronous Transfer Mode) network for the LHC will bepresented. ATM end nodes in the network are VME based PowerPC boardsrunning LynxOS. The ATM interfaces (based on the IDT 77201/77211 chip)are PMC modules that are accessed via the PCI bus using low latencychained DMAs. Zero copy data transfers from and to host memory space areused to accelerate the transmission and reception process. In a starlikenetwork topology like envisaged for the LHC, upstream AAL5 traffic atConstant Bit Rate to a central node is free of contention. Continuouserror free transfer rates up to the bit carrier frequency (155 Mbps)have been achieved. At the central node, an efficient dynamic storagesystem ('MOPS') was used to provided smooth data access to and from userspace. Down stream traffic is generated using ATM multicasting at theswitch level. It will be shown that ATM could provide anMultiple-Input-Multiple-Output (MIMO) infrastructure with a controlledcommunications latency like required for real time feedback control ofparameters like tune and the global orbit in the LHC.