Status of the FLASH Free Electron Laser Control System

Kay Rehlich

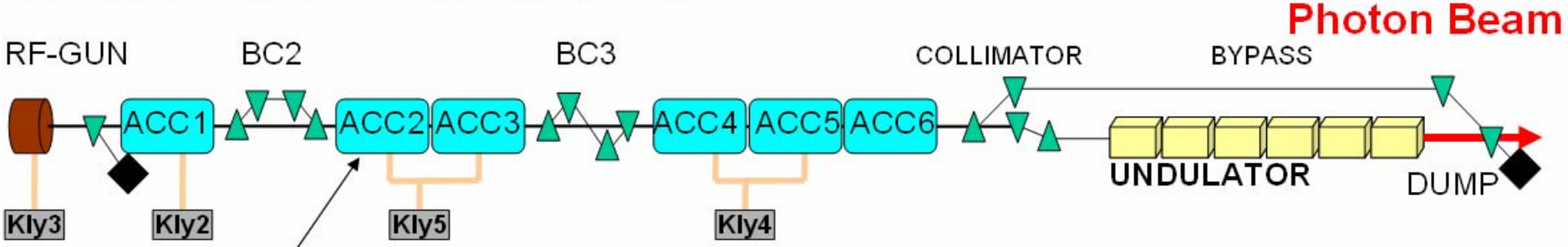
DESY

Content:

- **Introduction**
- **Architecture**
- **Future developments for XFEL**

FLASH

Energy:	0.4 .. 1 GeV
Peak current:	1-2kA
Wave length:	32 .. 6 nm
Photon:	$6*10^{15}$ W/cm^2



6 Cryo Modules
with 8 Superconducting Cavities each
1.3 Ghz

250m

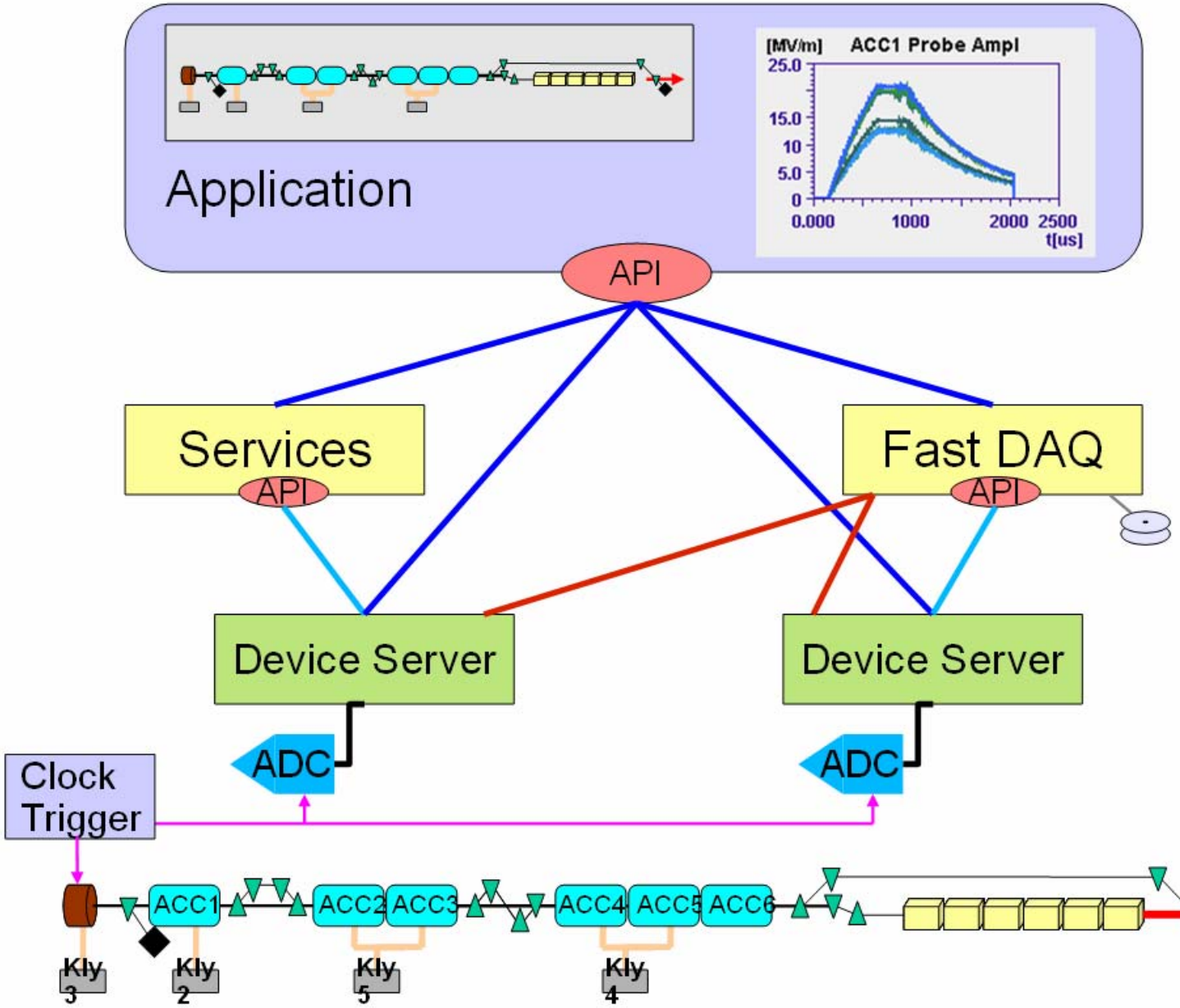
XFEL Project started 2007: 20GeV, 0.1nm, 3 km

Motivation

A Challenge for new Linear Accelerators:

- Provide **bunch synchronous distributed data processing** for ADCs and Images for the **accelerator** and the **experiments**

DOOCS Architecture



User Interface

Middle Layer

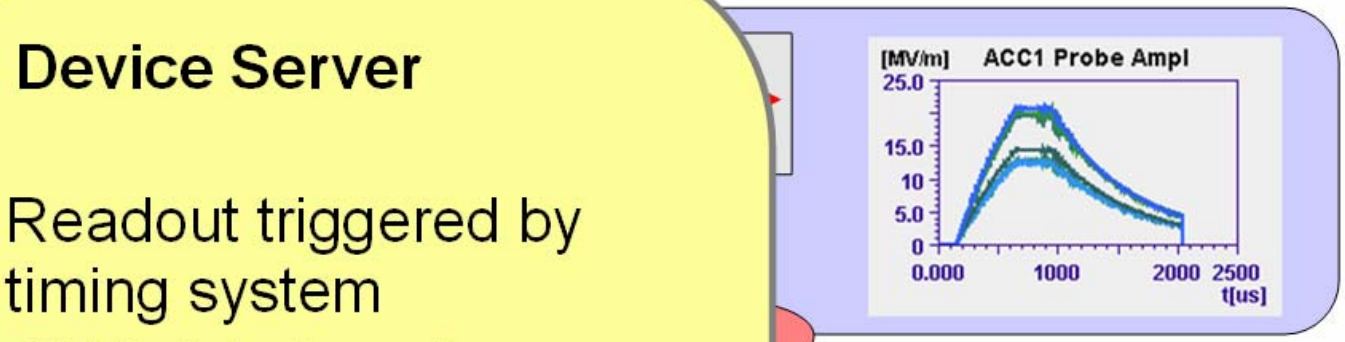
Front-end Tier

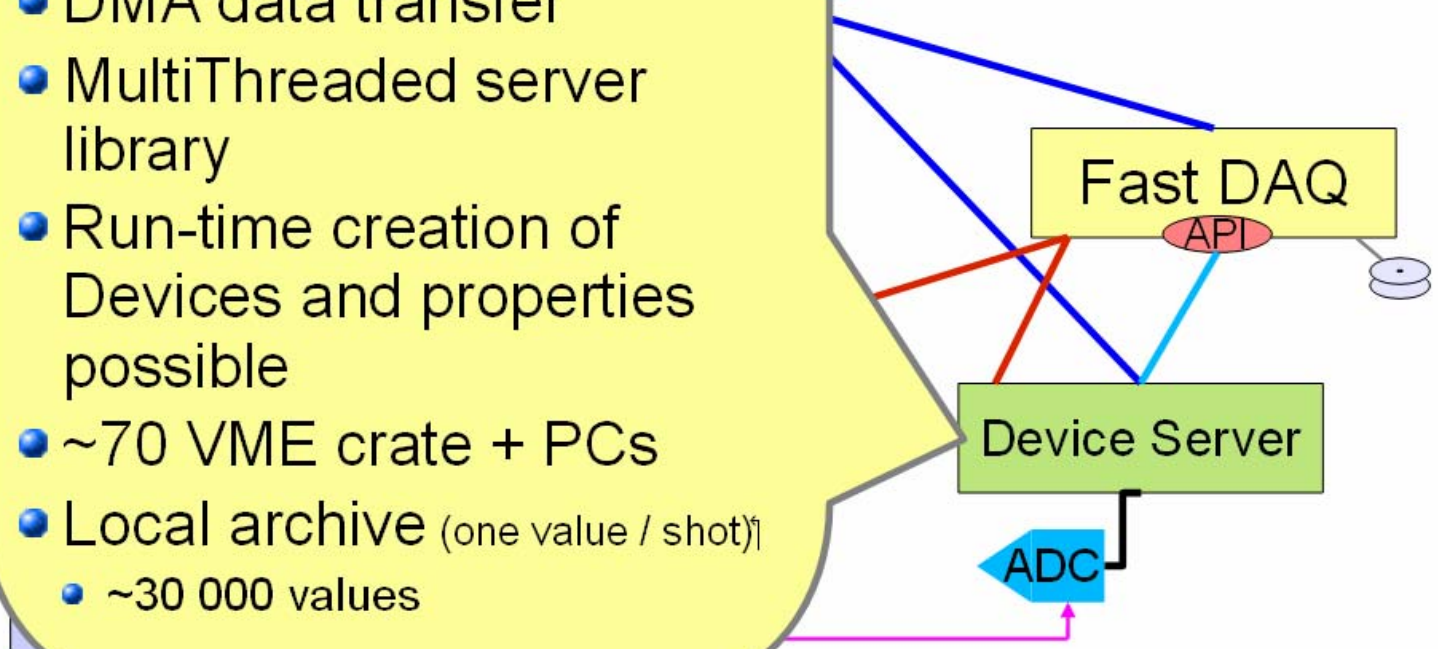
Accelerator, Experiments

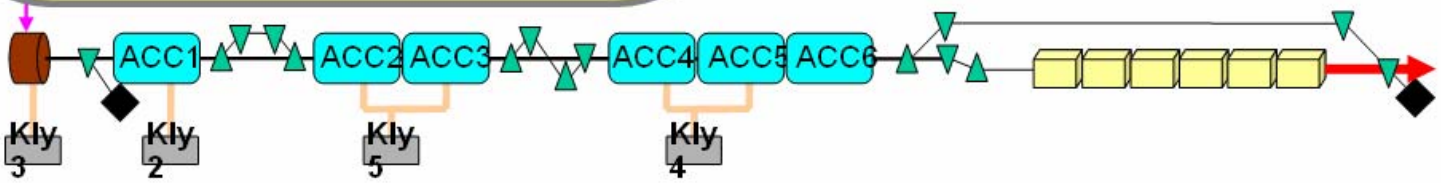
The Front-end

Device Server

- Readout triggered by timing system
- DMA data transfer
- MultiThreaded server library
- Run-time creation of Devices and properties possible
- ~70 VME crate + PCs
- Local archive (one value / shot)
  - ~30 000 values







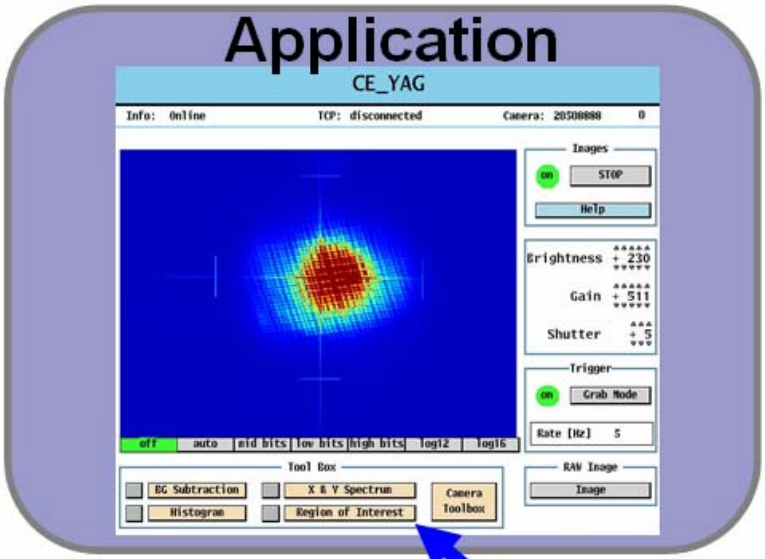
User Interface

Middle Layer

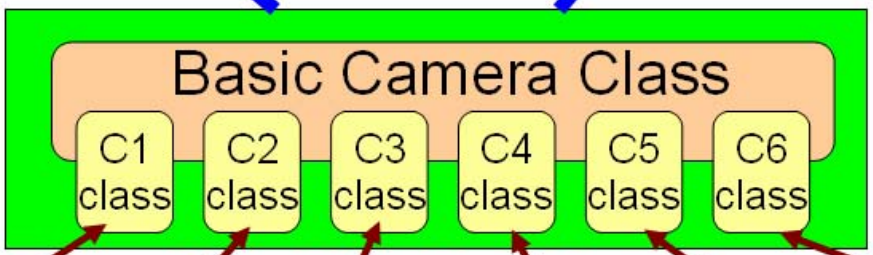
Front-end Tier

Accelerator, Experiments

DOOCS Camera Environment

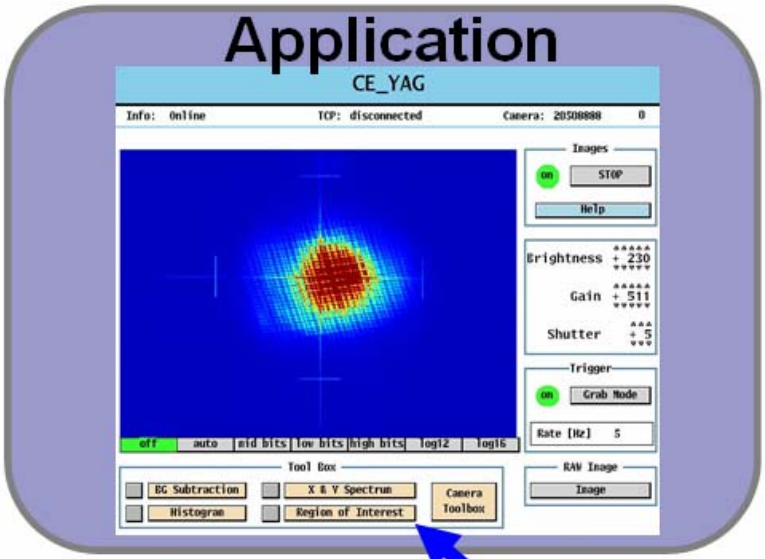


DOOCS Camera Server



USB FireWire Ethernet FrameGrabber

DOOCS Camera Environment



Poster: Wednesday

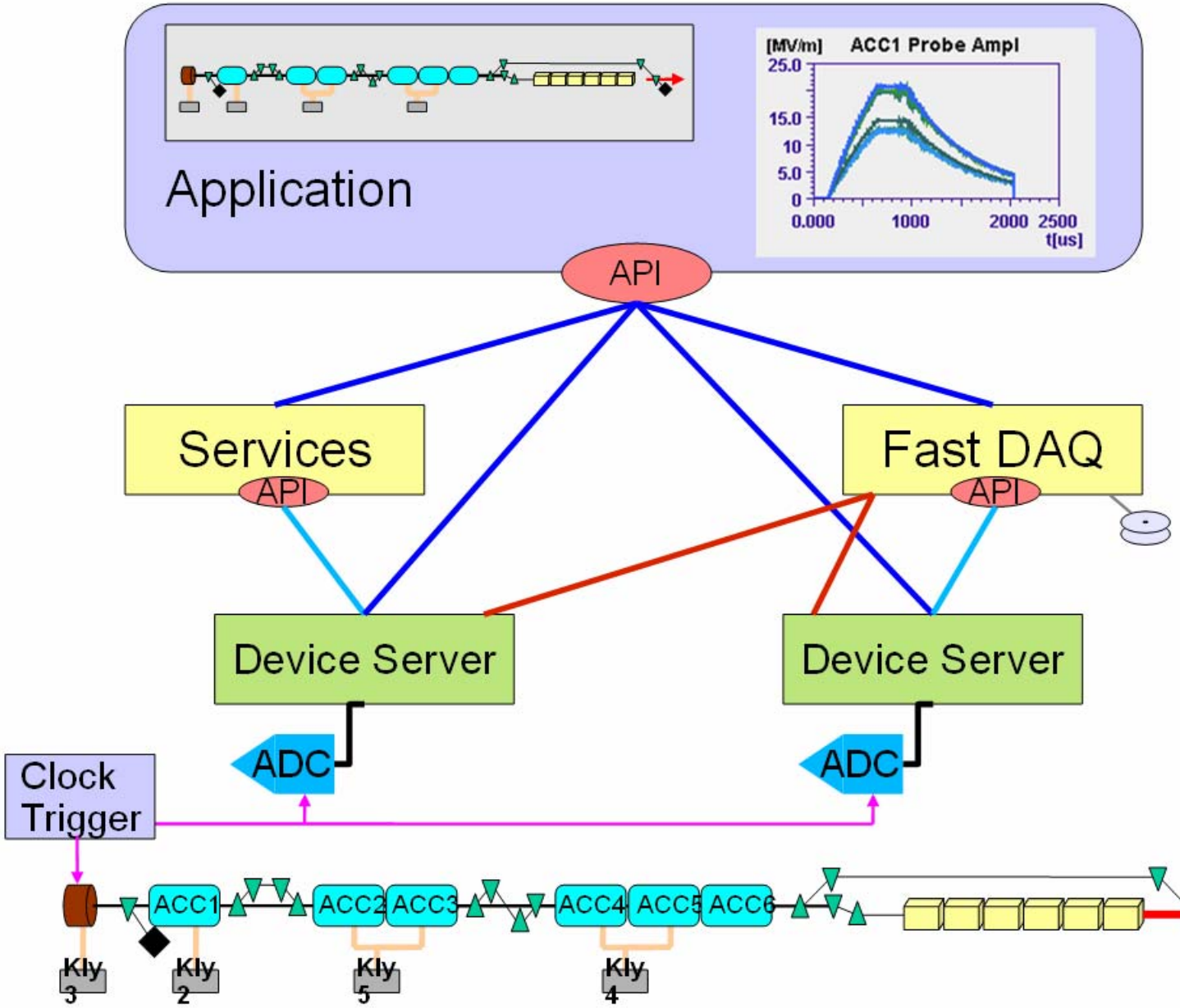
DOOCS Camera Server

Basic Camera Class

C1 class | C2 class | C3 class | C4 class | C5 class | C6 class

USB | FireWire | Ethernet | FrameGrabber

The Service Tier



User Interface

Middle Layer

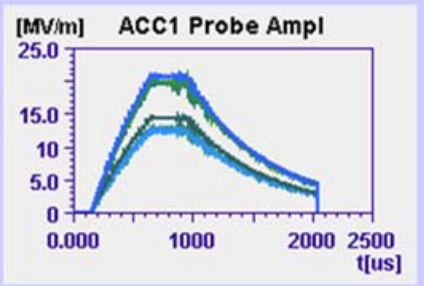
Front-end Tier

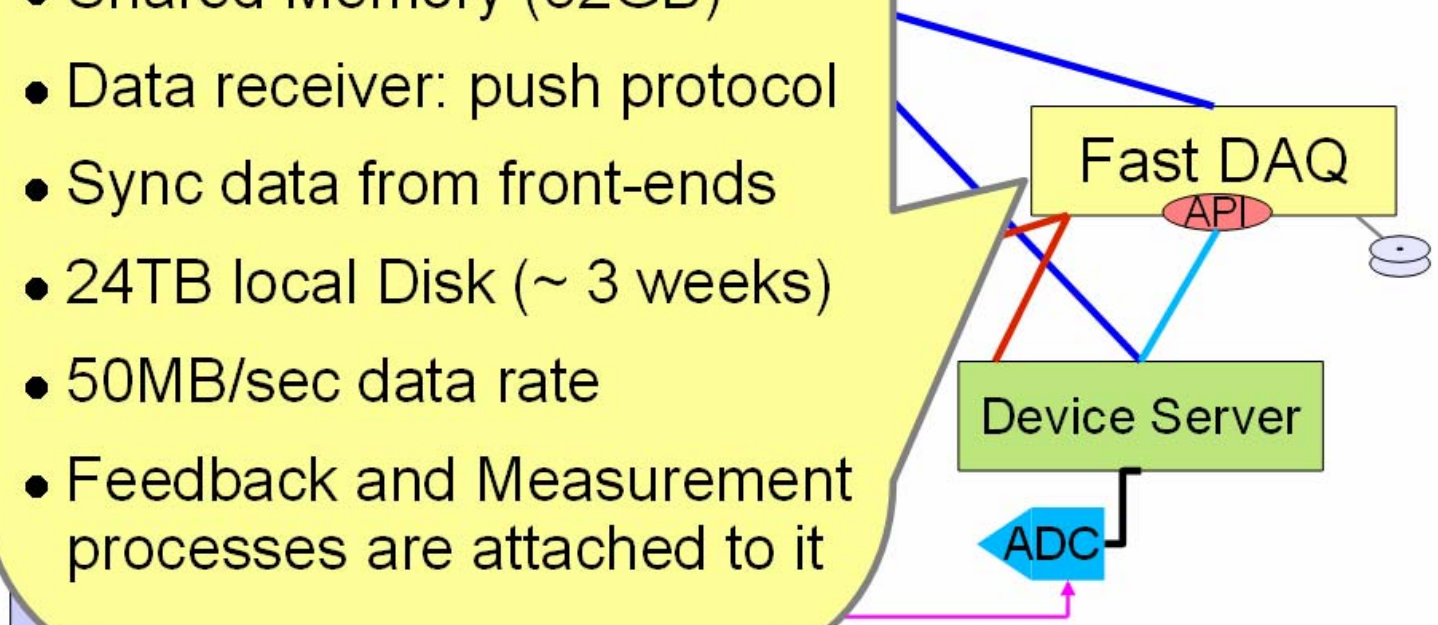
Accelerator, Experiments

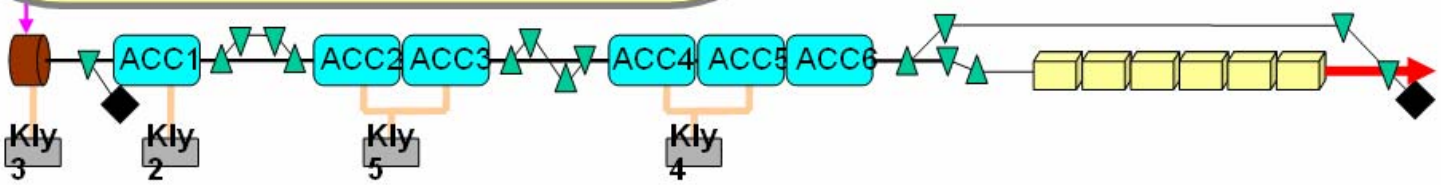
The Service Tier

Fast DataAQuisition System

- MultiThreaded
- Multiprocessor (16 CPUs)
- Shared Memory (32GB)
- Data receiver: push protocol
- Sync data from front-ends
- 24TB local Disk (~ 3 weeks)
- 50MB/sec data rate
- Feedback and Measurement processes are attached to it







User Interface

Middle Layer

Front-end Tier

Accelerator, Experiments

The Service Tier

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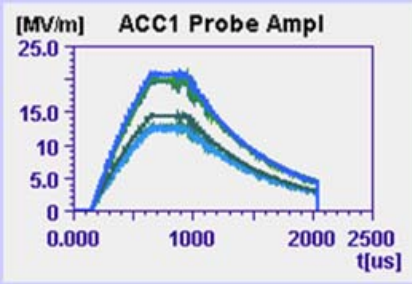


Poster: Thursday

Fast DAQ

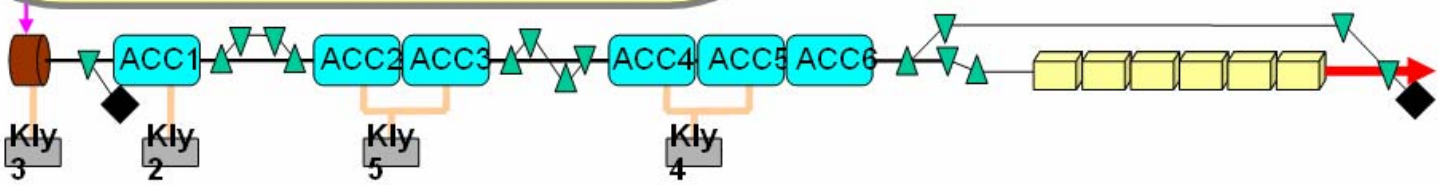
API

Middle Layer

Device Server

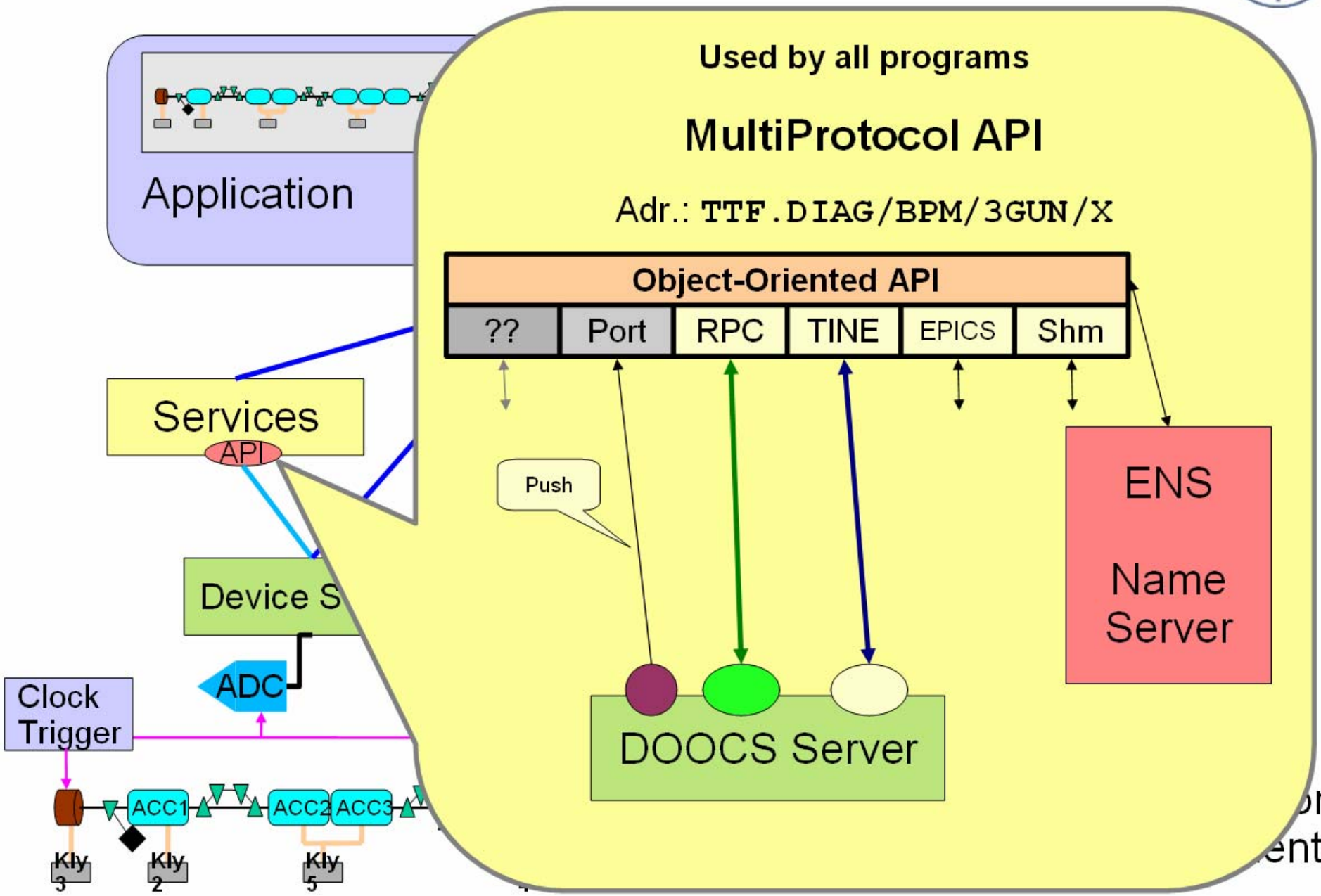
Front-end Tier

ADC



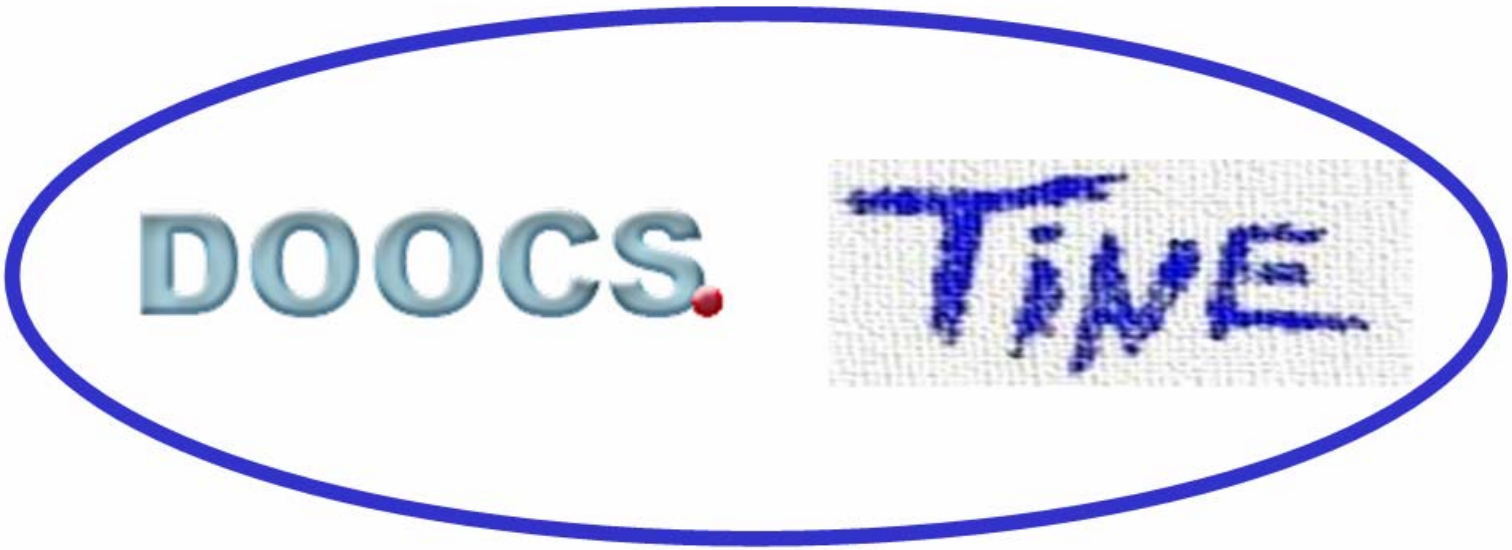
Accelerator, Experiments

The Protocols



DESY Control Groups

- The two accelerator control groups joined together

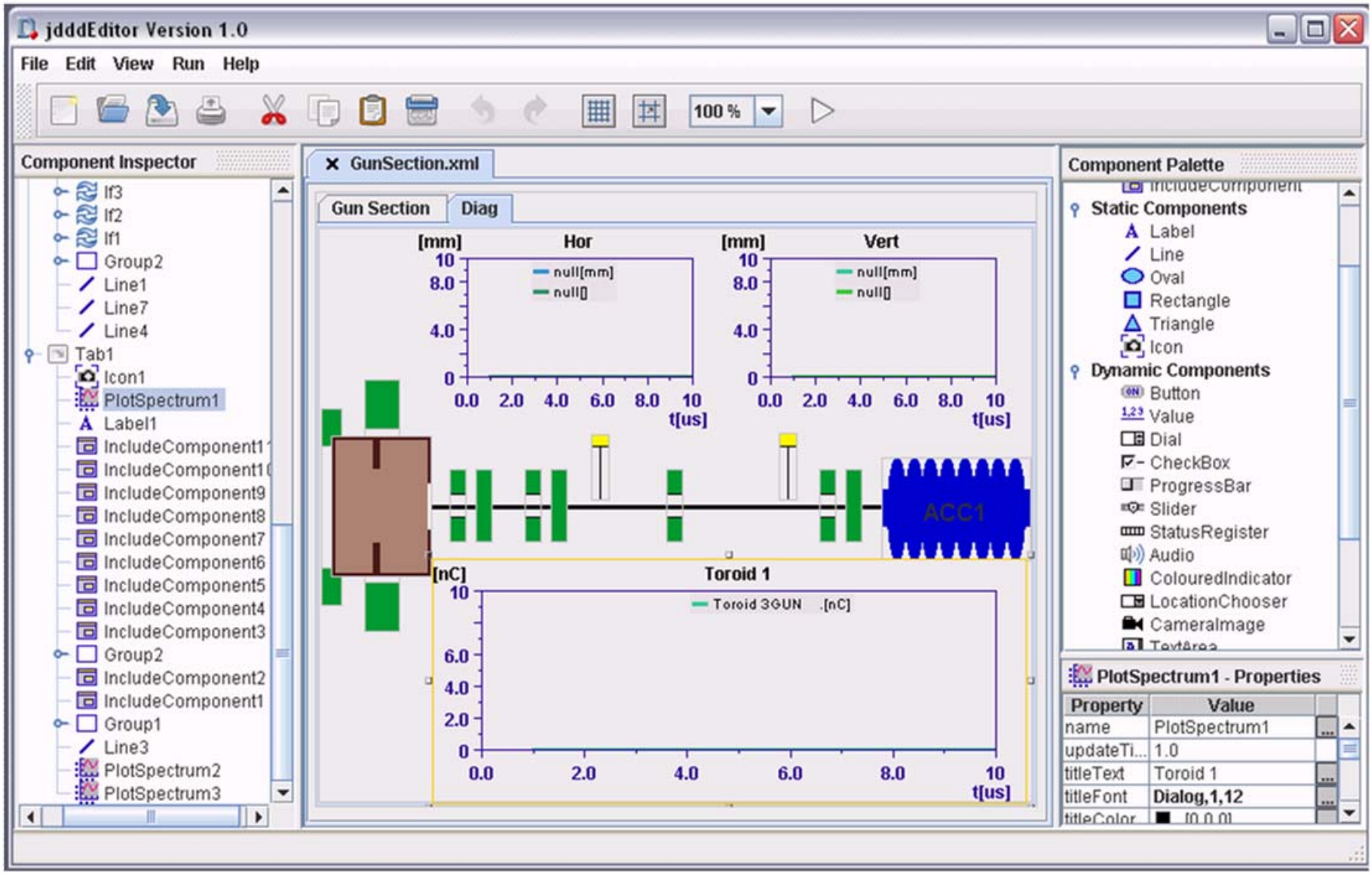


- Goal: benefit from the complementary strength of DOOCS and TINE

XFEL Developments

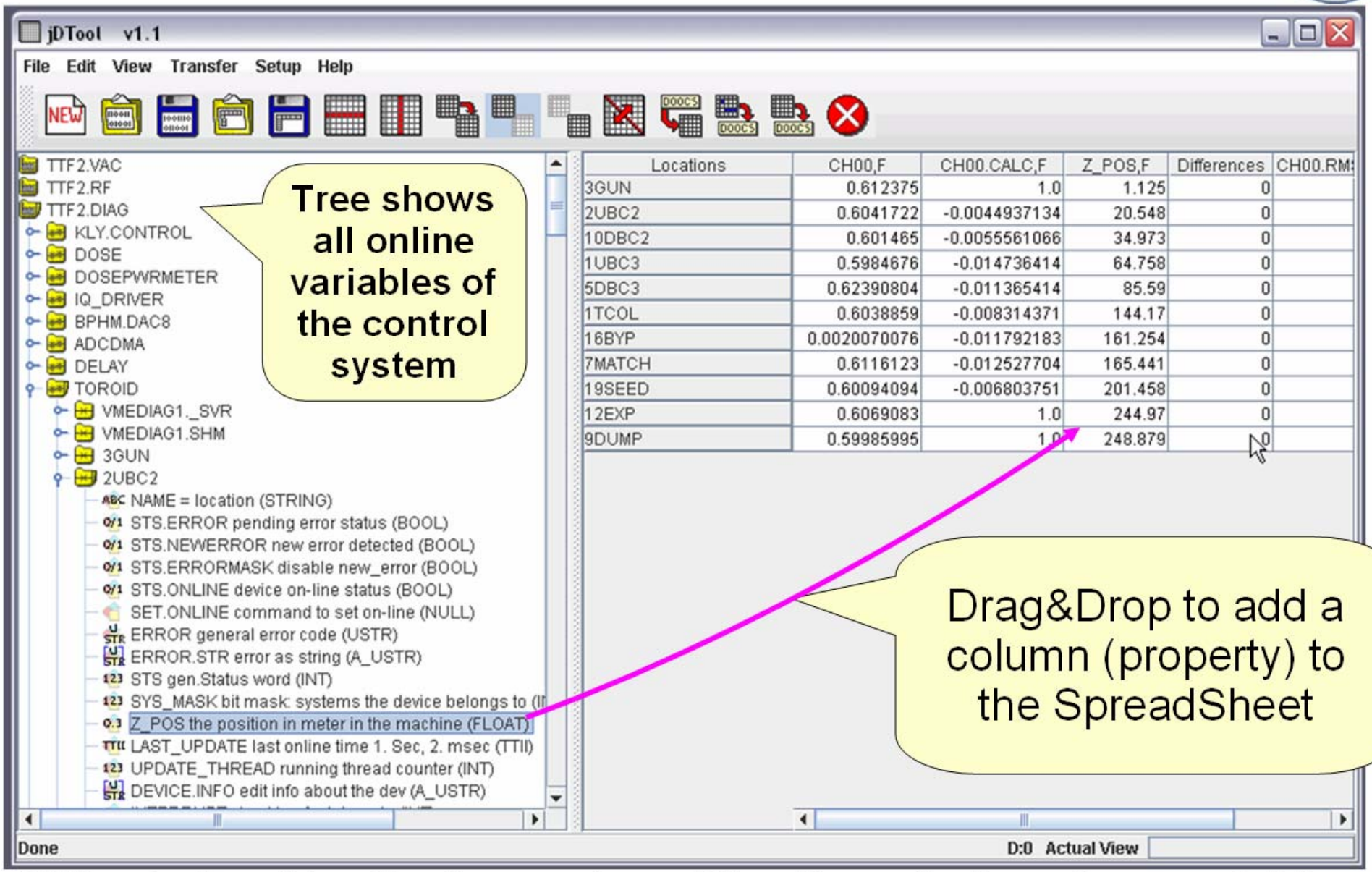
- GUI software based on JAVA
  - 3 projects
- Evaluation of a new crate standard: ATCA / µTCA
  - Modern GigaLink communication (no bus)
  - Redundant design (up to 99.999% availability)
  - Management infrastructure is part of the specification
    - IPMI on board and crate level
- DOOCS server development
  - Management server and display
  - Redundant device server or subsystem operation

The Applications: jddd



jddd: data presentation, controls and analysis framework
to create complex operation panels without programming

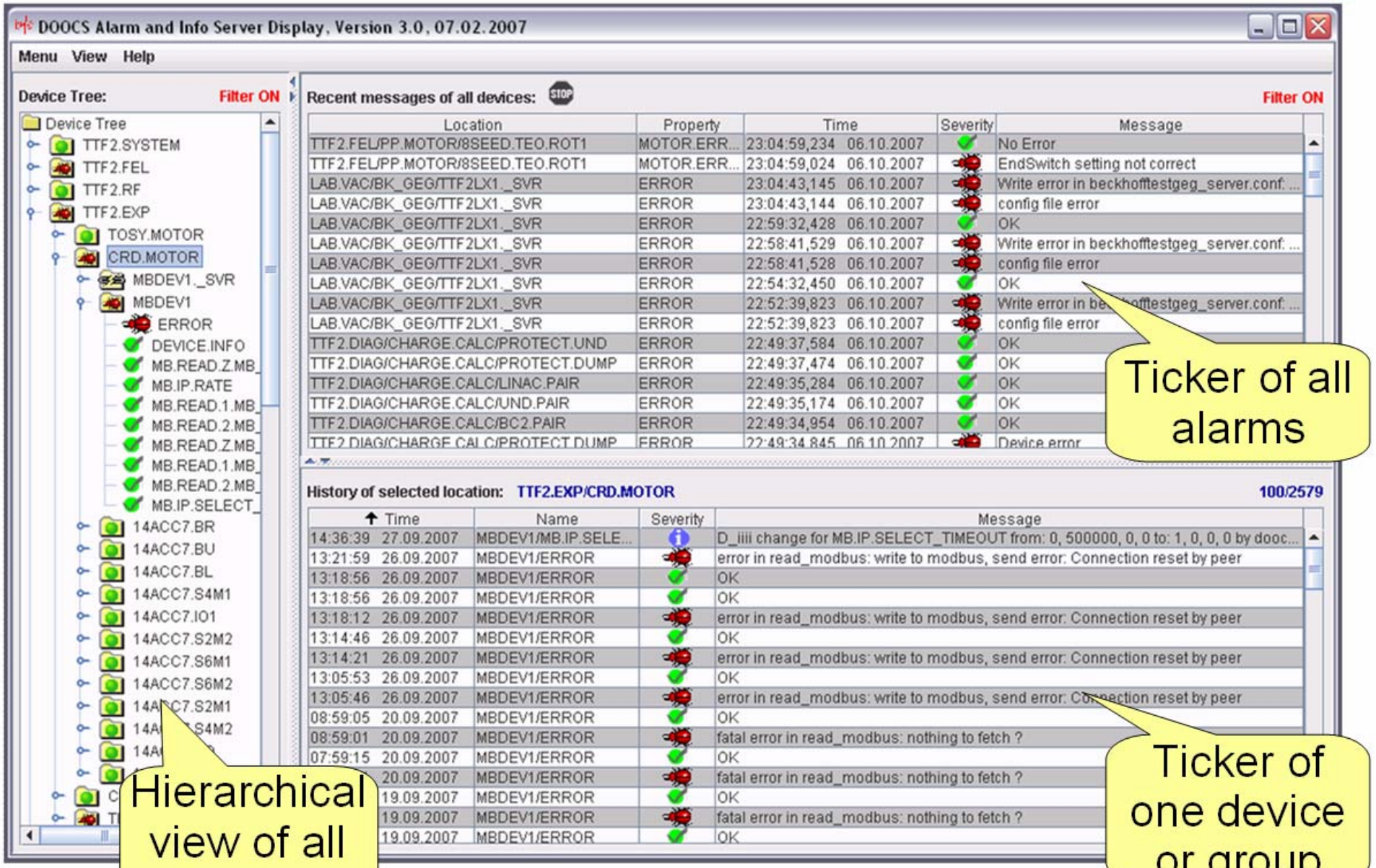
Data Browser



jDTool: Tool to display and modify all control system variables

FLASH
Free Electron Laser in Hamburg

Alarm Display

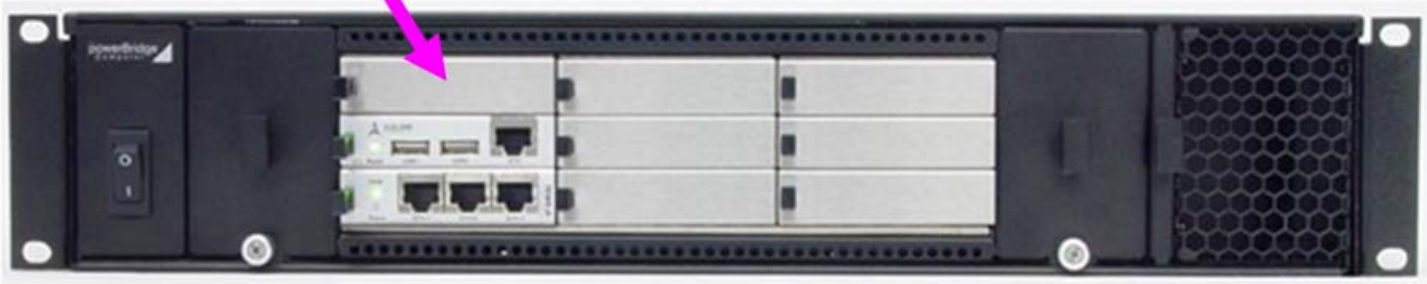


ATCA/µTCA Family

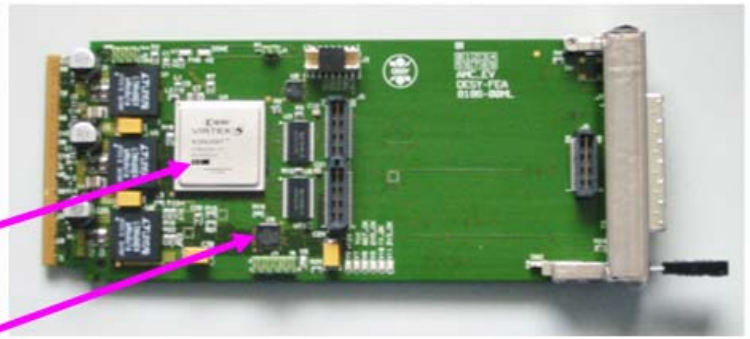
AdvancedMC™

AdvancedTCA®

µTCA™



Hardware Developments



- AMC modules
  - Universal, Virtex 5 FPGA, I/O piggy-back ☑ready
    - IPMI code for MMC (Module Management Controller)
    - PCIexpress interface to DOOCS
  - 8 channel ADC, 14bit, 100MHz ordered
    - Commercial product, ready this month
  - Timing system (ps stability) planned
  - Machine Protection System planned

Chassis Management @ DOOCS

Application

Display:
- Inserted modules
- Voltages
- Temperatures
- Fans

Function:
- On/Off
- Reset

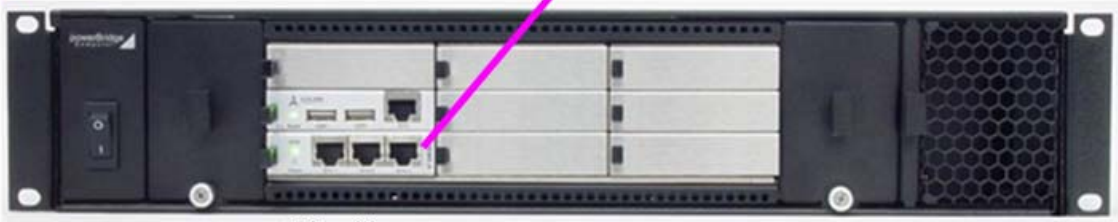
API

DOOCS Crate Server

Camera PC

IPMI over Ethernet

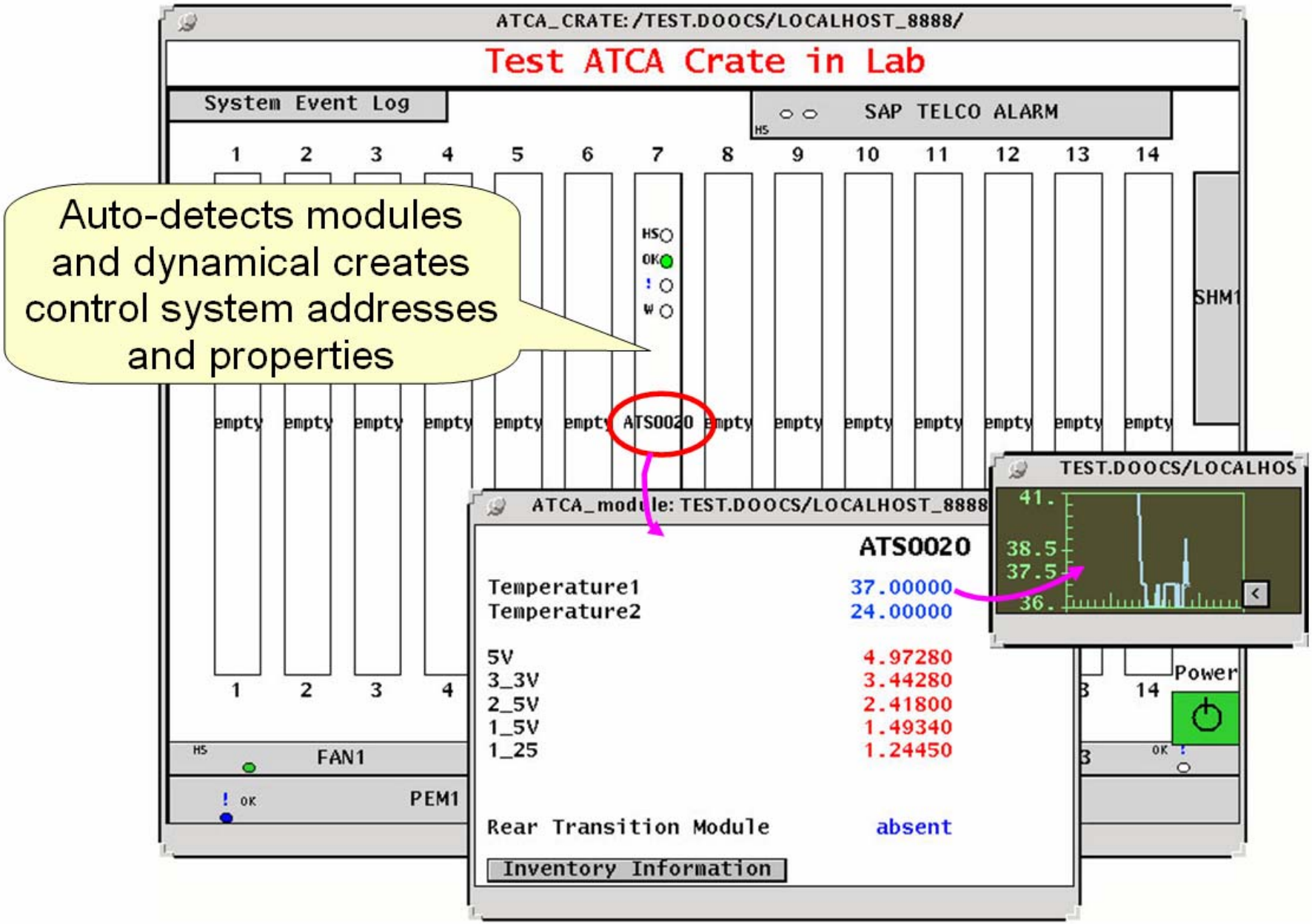
µTCA™



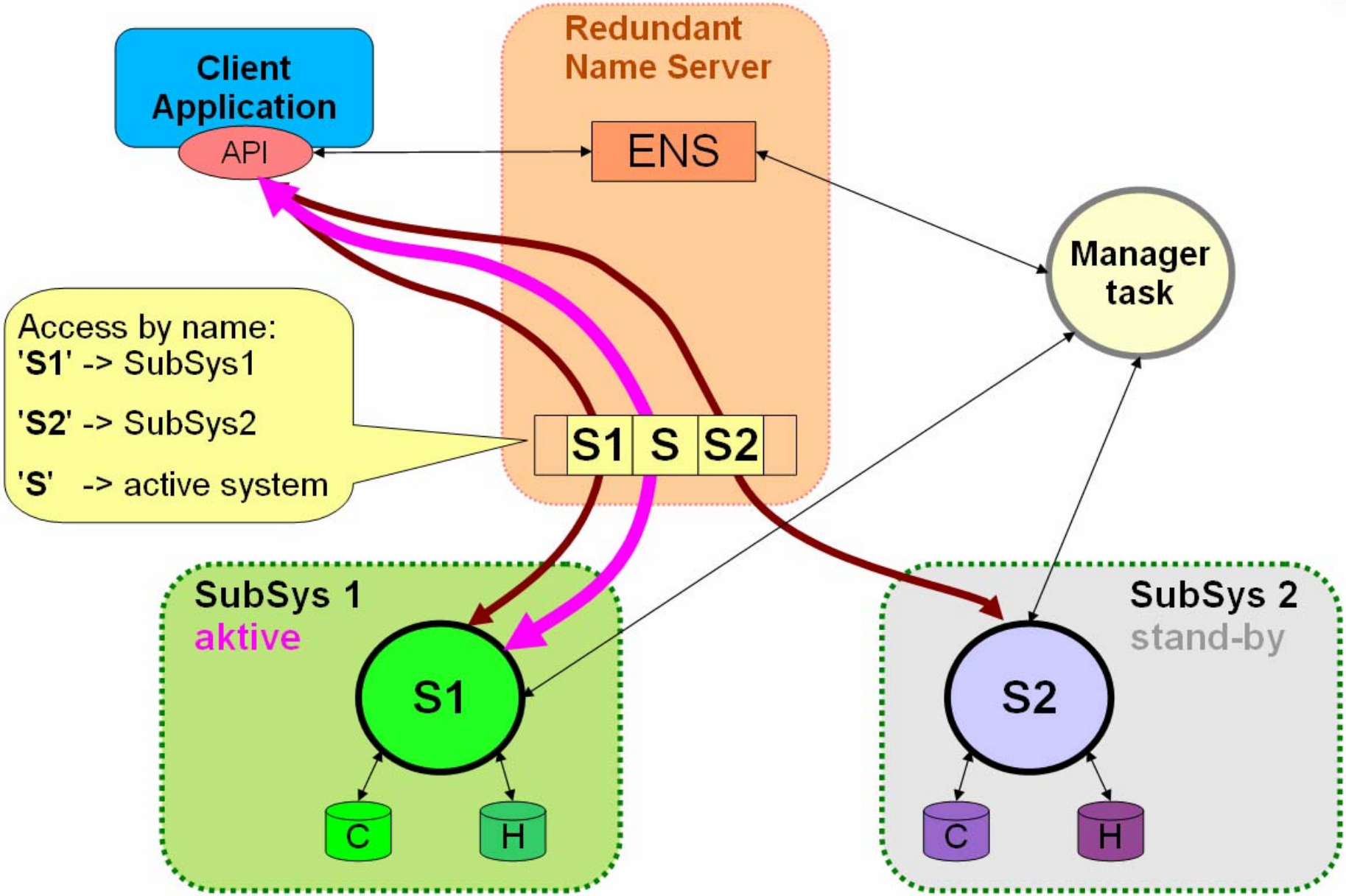
Shelf manager

AdvancedTCA

Chassis Management @ DOOCS



Redundant Server



Summary

- **FLASH: First SASE in January 2005**
  - **Now: 1GeV, 6.5 nm**
- **DOOCS @ FLASH:**
  - **Synchronous, high performance data recording**
  - **Runs reliable and is flexible / dynamic**
- **XFEL developments:**
  - **First JAVA applications**
  - **Evaluation of ATCA / µTCA crate standard**
  - **Implementation for management and improved availability**

More info: http://doocs.desy.de