

LCLS BEAM-POSITION MONITOR DATA ACQUISITION SYSTEM

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Abstract

In order to determine the transverse LCLS beam position from the signals induced by the beam in four stripline pickup electrodes, the BPM electronics have to process four concurrent short RF bursts with a dynamic range > 60 dB. An analog front end conditions the signals for subsequent acquisition with a waveform digitizer and also provides a calibration tone that can be injected into the system in order to compensate for gain variations and drift. Timing of the calibration pulser and switches, as well as control of various programmable attenuators, is provided by an FPGA. Because no COTS waveform digitizer with the desired performance (> 14 bit, ≥ 119 MSPS) was available, the PAD digitizer (see separate contribution [1]) was selected. It turned out that the combination of a waveform digitizer with a low-end embedded CPU running a real-time OS (RTEMS [4]) and control system (EPICS [3]) is extremely flexible and could very easily be customized for our application. However, in order to meet the BPM real-time needs (readings in < 1 ms), a second Ethernet interface was added to the PAD so that waveforms can be shipped, circumventing the ordinary TCP/IP stack, on a dedicated link.

INTRODUCTION

In the *Linac Coherent Light Source* (LCLS) very short electron bunches pass an arrangement of 4 stripline electrodes [2] nearly at the speed of light inducing a doublet of short pulses at the upstream stripline terminal (fig. 1; red curve). The sensitivity of the pulse amplitude to transverse beam position is $\delta A/A \approx 2\delta r/R$. Combining the resolution requirement of $\approx 10\mu\text{m}$ with a BPM radius of $R \approx 10$ mm and some headroom for accommodating beam charge and offset variations it follows that the data acquisition system must have a dynamic range of 60 – 80 dB. The dynamic range is limited by a number of parameters such as noise figure, bandwidth, distortion, digitizer resolution etc. which all must be carefully tuned to achieve optimal performance.

SYSTEM OVERVIEW

The LCLS BPM data acquisition system (fig. 2) consists of a front-end electronics module (AFE), an intelligent waveform digitizer (PAD), several network links and a VME computer (IOC) that integrates the BPMs with the EPICS [3] control and timing systems.

One AFE + PAD provide four channels to simultaneously condition and digitize all pickup signals of a single BPM using an internal digitizer clock. A beam-

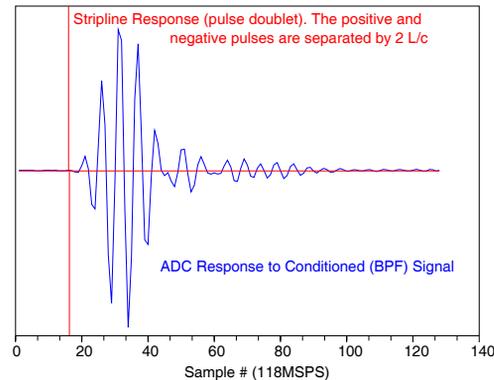


Figure 1: BPM Signal and Typical AFE/ADC Response. On the timescale of the digitizer the pulse doublet (red) cannot be resolved (the LCLS stripline length is $\approx L = 5 - 6''$). The band-pass filtered AFE response has a greatly reduced amplitude but is stretched out in the time-domain.

synchronous trigger is distributed by the timing system and delivered by a VME card (“EVR”) that is housed with the IOC. Fig. 1 (blue curve) shows the typical digitized response of the acquisition system to the raw stripline signal (red curve).

The PAD digitizer features an embedded low-end CPU which forwards the raw waveform data over a dedicated network link to the IOC and performs low-priority house-keeping tasks. Slow controls and monitoring is possible via TCP/IP over the primary network interface (IF1).

A distinct feature of the system is an on-line calibration facility to determine imbalances in the vertical (A, D) and horizontal (B, C) signal paths, respectively. Two calibration cycles are interleaved in time between “real” beam pulses; hence at the maximal LCLS beam rate of 120 Hz the BPM data acquisition actually runs at 360 Hz.

Multiple BPM electronics are connected by means of an ethernet switch to one single IOC where the raw waveforms are processed and bunch-by-bunch position is calculated for all attached BPMs. The data are timestamped and passed up a stack of higher-level software layers which provide additional processing such as averaging, buffering etc. EPICS interfaces to the different layers are provided.

ANALOG FRONT END

The AFE sets the signal frequency, bandwidth and level using appropriate filtering and low-noise programmable gain stages.

A tone generator, power-amplifier and a circuit of solid-state analog switches implement the calibration tone injector. The switching state machine and timing are con-

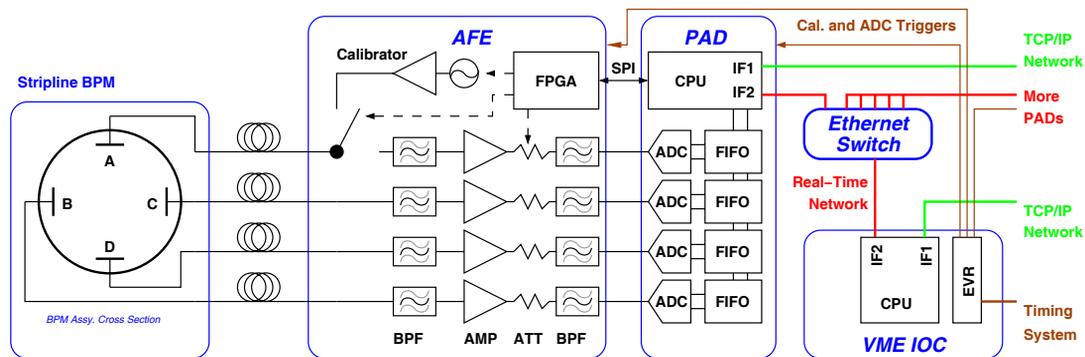


Figure 2: System Block Diagram. Note that the switches for injection of the calibration tone into C for calibrating the vertical channel pair A, D have been omitted for sake of simplifying the schematic.

trolled by logic in a FPGA-device which also provides a simple programming interface for the calibrator and AFE programmable attenuators via a SPI port.

Gain Stages and Filtering

The AFE confines the signal bandwidth to ≈ 10 MHz around a processing frequency $f_c = 140$ MHz and provides gain to increase the signal to a level suitable for the digitizer.

Programmable attenuators in various stages permit on-line tuning of the signal levels into the ADC. The calibrator level can also be adjusted.

The processing frequency was chosen so that it falls well within the ADC signal bandwidth (ADC performance suffers with increasing f_c) but high enough for sufficient available signal power (pulse doublet frequency response is zero at $f_c = 0$). Also, for the calibration method to work, zeros in the stripline cross-coupling response must be avoided¹.

The choice of bandwidth is also a trade-off. While the SNR in the AFE increases with bandwidth, digital processing gain due to oversampling decreases. Obviously, the choice of bandwidth is also constrained by the Nyquist frequency of the ADC.

Due to the very wide bandwidth of the stripline signals early filtering is paramount² to avoid distortion in the gain stages. An anti-alias filter at the output of the AFE eliminates wideband noise generated and amplified by the gain blocks.

On-Line Calibration

The AFE can send a calibration tone on one cable, e.g., A upstream to the stripline assembly where due to the inherent cross-coupling between strips the tone couples to adjacent channels B and C where it is received and digitized by the AFE/PAD. Provided that the coupling ra-

tio $(B/A)/(C/A)$ remains constant, determining the ratio $g_{cal} = B_{cal}/C_{cal}$ of the calibration tone levels at the outputs of channels B and C allows for calibrating against any imbalance in the cabling plant, AFE gain drift etc.

Likewise the calibrator can emit its tone on channel C in order to calibrate the “vertical” signal paths A and D .

Note that knowledge of g_{cal} is all that is required since (horizontal) position information is reflected in the amplitude ratio of channels B/C and often extracted in the form $(B - C)/(B + C)$.

DIGITIZER

A four-channel “PAD” digitizer [1] is employed for digitizing the signals coming out of the AFE at a sampling rate of 118 Mhz, i.e., *undersampling* the third Nyquist zone. The samples are written into FIFO-devices upon reception of an external trigger which is provided by the timing-system and synchronous with beam arrival.

The PAD embedded CPU features a SPI interface which is used to control the AFE calibrator and attenuators. The PAD can operate in stand-alone mode providing EPICS controls of the various features and access to the waveforms transferred out of the FIFOs which is very useful in a laboratory environment.

However, due to the limited processing power of the PAD-CPU and the inherently non-deterministic nature of ethernet and TCP/IP in particular it was determined that EPICS and the network stack would not be adequate to deliver BPM readings under a real-time constraint of < 1 -ms response time³.

Therefore, hardware for a second 100-baseT ethernet interface (IF2) was added to the PAD design thus opening a path for real-time critical communication where BPM waveform data can be streamed into a more powerful computer over a dedicated network without any ordinary TCP/IP activity.

¹It can be shown that zeros coincide with the maxima (and zeros) of the signal spectral response.

²This is a case where cable losses – the BPM striplines are located at ≈ 150 ft from the electronics – actually are beneficial helping to reduce high-frequency signal power

³The timing requirements are such that BPM readings must be made available to higher-level software (such as feedbacks) in less than 1 ms. This budget includes FIFO readout, data transmission and complete processing.

Using the RTEMS hard real-time OS [4] on the PAD makes it possible to have a high priority task copying 4×128 samples (totaling ≈ 1 kB) out of the FIFOs and sending them through the IF2. This task also controls the calibration cycles that are interleaved between beam pulses.

Any other activity (including slow EPICS controls and monitoring of the PAD) occurs at a lower priority without impact on the critical data stream.

COMMUNICATION AND DATA PROCESSING

A simple protocol stack was developed for communication over ethernet between the main IOC and the PADs: The IOC broadcasts a “request packet” to all PADs and these then send a reply back to the IOC. The replies are buffered in an ethernet switch and “concentrated” into one 1-Gb uplink to the IOC. This simple scheme avoids the need for address lookup so that any activity on the link is completely deterministic. This “real-time” protocol stack (RTS) runs with a high priority on a real-time OS (RTEMS). The RTS implementation is completely independent from the ordinary TCP/IP stack — no coupling or routing of any type between the stacks whatsoever exists.

However, the BPM real-time protocol is actually layered on top of traditional IP and UDP headers and trivial implementations (no fragmentation, no routing etc.) of these protocols (and even some optional ARP and ICMP functionality) are provided by the “real-time stack”.

This makes it possible to develop and test the RTS on a ordinary network in combination with standard TCP/IP software and tools (of course, deterministic response time is not available in such an environment). Since the API to the RTS is very similar to the well-known UDP sockets the RTS is easy to use.

To gain deterministic behavior, instances of the RTS execute on the IOC and all PADs using IF2⁴ hardware and a dedicated ethernet segment.

Driven by the timing system, the IOC broadcasts requests (for data or calibration cycles) at 360 Hz⁵ and receives the requested beam or calibration data in return. The IOC also embeds timestamp information (to which the PAD CPUs have no direct access because no hardware for interfacing to the timing system is included on the PAD) and beam charge announcements with the requests so that the PAD CPUs can tag data and update AFE attenuator settings from pulse to pulse.

The IOC’s RTS listens on its IF2 for PAD replies and processes the incoming waveforms calculating calibration parameters and position. It provides a variety of EPICS PVs for diagnostic purposes. The raw positional data are

passed to other EPICS software modules hosted on the IOC which implement higher level services such as averaging, buffering etc. but which shall not be further discussed here.

The IOC also is equipped with a “EVR” (Timing System Event Receiver) module and driver software that integrate the IOC with the global LCLS timing system. The EVR provides the necessary hardware triggers for the calibrator and PAD data acquisition. The exact trigger time can be adjusted individually for every signal under software control.

SUMMARY

Acting from necessity, the existing PAD design which had originally been developed for the LCLS low-level RF was adopted for the LCLS BPM project, enhancing it with a second ethernet interface. On the software side, a special real-time protocol stack was developed enabling us to read the PAD digitizers/FIFOs and stream raw waveform data into a powerful VME computer which produces position readings within the required time frame of 1 ms.

The combination of PAD and RTS has proved to be quite generic and has been or will be adopted for other applications.

Employing the PAD and RTS in combination with the RTEMS real-time operating system and EPICS allowed us to develop the BPM data acquisition software in about 6 months and to deliver it timely for LCLS injector commissioning with the expected performance.

REFERENCES

- [1] Dayle Kotturi, Ron Akre, Till Straumann, “130-MHz, 16-Bit Four-Channel Digitizer,” ICALEPCS’07, Knoxville, October 2007.
- [2] R. Shafer, “Beam Position Monitoring”, AIP Conf. Proceedings on Accelerator Instrumentation, Upton, NY, 1989.
- [3] “Experimental Physics and Industrial Control System,” <http://www.aps.anl.gov/epics/>.
- [4] “Real-Time Operating System for Multiprocessor Systems”, <http://www.rtems.com/>.

⁴The IOC also features a second interface and a RTS driver

⁵Note that the precise timing for data acquisition is achieved by using hardware trigger signals from the timing system that connect directly to the PAD FIFOs and AFE calibrator. The “request packets” just provide setup and timestamp information.