130-MHz, 16-BIT FOUR-CHANNEL DIGITIZER*

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Abstract

The PAD (Phase and Amplitude Detector) was designed to digitize high-speed analog input data with large dynamic range. Because of its high speed and high resolution processing capability, it has been useful to applications beyond measuring phase and amplitude of RF signals and klystron beam voltages. These applications include beam-position monitors, bunch-length monitors, and beam-charge monitors. For each channel, the 16-bit digitized signal is clocked into a 64k sample FIFO. Commercial FIFOs are available that store up to 256k samples in the same package. The data are then read from the FIFO into the Arcturus Coldfire uCDIMM. A CPLD is used to handle triggering, resetting the FIFO, interfacing the processor to the 4 FIFOs, and interrupting the processor. The processor runs RTEMS version 4.7 and EPICS 3.14.8.2. There is an optional add-on available that attaches to the QSPI port on the PAD for reading 8 slow, 24-bit analog signals.

INTRODUCTION

The digitizer used is the Linear Technologies LTC2208. Introduced in the summer of 2006, it was the first 16-bit digitizer chip on the market capable of running at 119MHz; it is specified to run up to 130MHz. Initially a 2-channel board was to be built for the RF system, but the BPM requirements pushed the design to 4 channels.

The PAD clock is run at 102MHz which is 4 times the IF frequency. This makes down-conversion to DC multiplication by sines and cosines of multiples of 90 degrees, or ones and zeros. The LTC2208 has a built-in dither DAC circuit which varies the location along the ADC transfer function where the signal is digitized. Measuring low noise RF signals, especially CW signals digitized at a harmonic of the RF, can be hampered by nonlinearities in the ADC transfer function appearing as noise or errors which do not average out. By first adding in, and then digitally subtracting out this dithered signal, the nonlinearities in the ADC transfer function are averaged out.

The input transformers for the clock and signal paths to the LTC2208 were changed to 4:1 impedance ratios to reduce input power levels. This had a slight reduction in SNR.

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Signal Input

The input signal for the ADC (Figure 1) uses a Minicircuits transformer to level shift the inputs to the ADC bias. The 20ohm, 18pf, input filter attenuates sample and hold transients coming out of the ADC and bandwidth limits the input. The TC1-1T limits the input frequency from 400 kHz to 500 MHz. The ADC is set to run at 2.25 Vpp, and the series resistors likely raise this another 5%, depending on frequency.

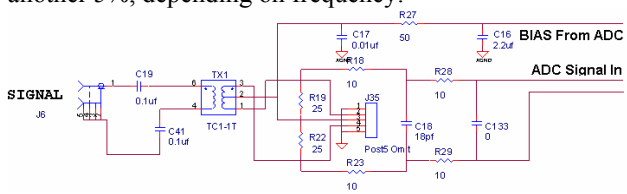

Figure 1: Input signal

Clock Input

The clock (Figure 2) is input to the board at 21dBm and split 6 ways. Each of the 6 signals is approximately 13dBm. Four of the signals drive the ADC with the above circuit. One of the clocks drives the CPLD, and another clock is routed to an SMA connector for off-board use. The clock rate of the ADC is specified to be between 1MHz and 130MHz. The board has been tested at 102MHz.

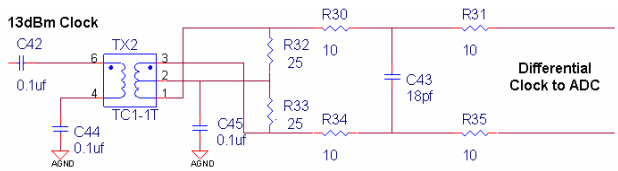

Figure 2: Clock signal

For each channel, the 16-bit digitized signal from the LTC2208 is clocked into a 64k-sample FIFO. Commercial FIFOs are available which store up to 256k-samples in the same package. The data is then read from the FIFO into the Arcturus Coldfire uCDIMM. A CPLD is used to handle triggering, resetting the FIFO, interfacing the Coldfire processor to the 4 FIFOs, and interrupting the Coldfire processor.

A block diagram of the digitizer is shown in Figure 3.

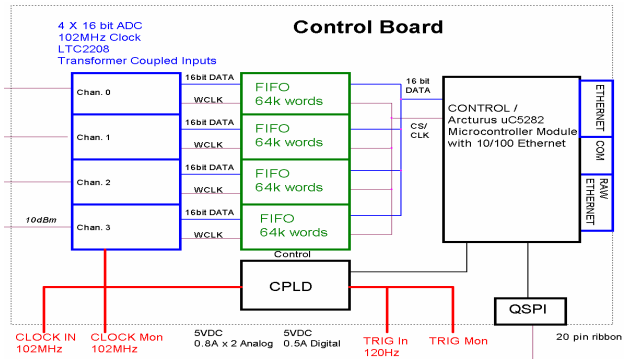

Figure 3: Block diagram of digitizer

FEATURES

- 4 Chan - 130MSPS 16 bit ADCs LTC2208 - Data clocked into 64k Sample FIFOs
- 1 buffered clock input to CPLD
- 1 buffered trigger input to CPLD
- 2 unbuffered coax I/O from CPLD
- 3 digital I/O from CPLD
- 4 interrupts to uCdimm5282
- Ethernet Port RJ45 connector
- 2nd Ethernet port using SMSC LAN9118 Ethernet Controller
- 1 COM Port to 9 pin D connector
- 1 COM Port to header
- I2C Port to header
- QSPI 4-wire Serial port with 4 chip selects to header
- 12 bit General Purpose I/O to header
- 6 10-bit MUX analog in or 4 digital I/O and 2 digital outs to header

A photograph of the digitizer is shown in Figure 4.

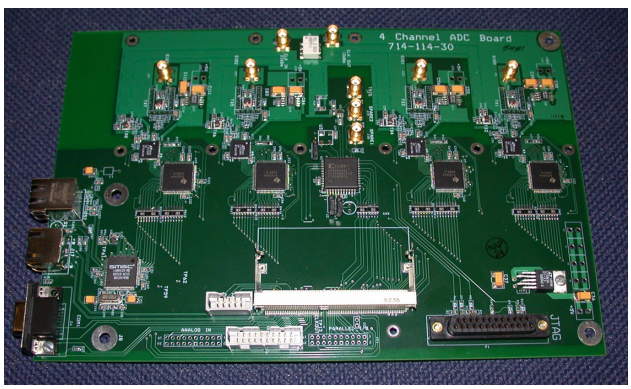

Figure 4: Preproduction prototype digitizer

PROCESSOR

The PAD processor is an Arcturus uCdimm Coldfire. It runs the RTEMS operating system, version 4.7.1 built for m68k target *uC5282* and EPICS, version 3.14.8.2, built for *RTEMS-uC5282* target.

CPLD

Interrupt pin 1 of the Arcturus module is connected to one input of an OR gate. The other input is connected to the Hardware trigger. A rising edge output of the OR gate sets a flip-flop high and starts the state generator. If either the hardware trigger or IRQ1 is held high, future inputs can not cause a low to high transition on the output of the OR gate and start the state generatoOnce the state generator is started, it can not be restarted until the flip-flop has been cleared. The following sequence occurs with the respect to the clock cycle after the trigger:

On trigger, one side of an AND gate to set FIFO_nREN goes high. The other side of the AND gate is high at this time, which causes FIFO_nREN to go high and disable reads. This must be done before a Master Reset on the FIFO. After two clock cycles, FIFO_nMRS (Master Reset) goes low and resets the FIFO. After 4 clock cycles, FIFO_nMRS goes high and the FIFO reset complete. After eight clock cycles, FIFO_nREN goes low enabling reads from the FIFO. FIFO_nWEN goes low enabling data to be clocked into the FIFO. IRQ2 goes low to generate an interrupt. A 20bit counter clear goes low to enable counting

Bit 1 of the counter (/4) generates a clock divide by 4 test signal which is gated by use of two 8 bit comparators on bits 2 to 9.

Bit 20 is used to disable the FIFO_nWEN, set IRQ2 high, and clear the trigger flip-flop. So after 524288 + 8 clocks the trigger is enabled. At 102MHz this is 5.14mS.

SLOW ADC OPTION

The digitizer supports the addition of an optional slow ADC board. It uses a Burr-Brown ADS1218, 8 channel, 24 bit, ADC. The data is read from the ADC through the QSPI port of the control board. The 8 analog channels are fed out through 2 RJ45 jacks. The board is shown in Figure 5.

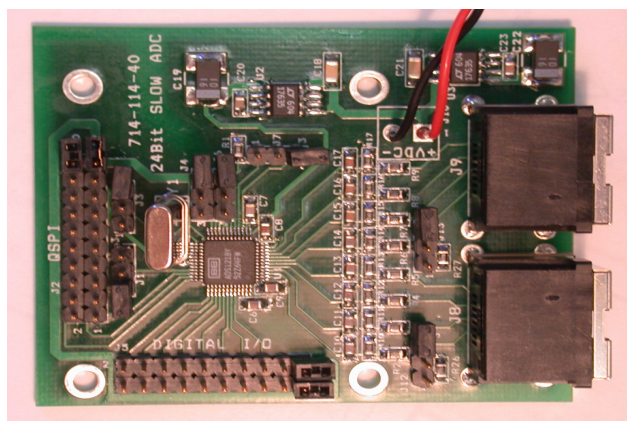

Figure 5: Slow ADC board

Using factory presets, we can achieve more than 20 effective bits.

The board has biasing for the AD590 temperature measuring device. The transfer function for this device is shown in figure 4, which gives 298.2uA + 1uA/degC. The 24bit ADC is reading the voltage across a 1.4k ohm resistor. With 20 effective bits over 2.5volt range the effective LSB is 2.4uV. 1uA/degC into 1.4k ohms is 1.4mV/degC. The effective temperature resolution of this device is 2e-3degC.

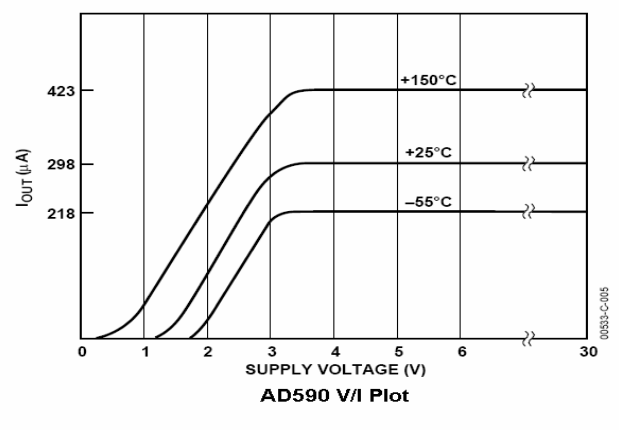

Figure 6: Transfer function for the AD590

SOFTWARE

With each trigger, an interrupt is seen by the processor. The interrupt service routine (ISR) is invoked and sets an event that another task is waiting on. The ISR increments a counter and is done. The task reads the FIFOs, first to the offset of the desired sample (this data is read but not stored) and then for each data point in the sample (this data is read and stored). Since different offsets, sample sizes and data processing algorithms are possible for each of the four channels, the FIFOs are read one at a time. This is not as efficient as reading all channels in a single loop, but necessary to meet the requirement that different offsets and sample sizes are possible.

To minimize the time needed to read and process the data, the copy of the data from the chip select register into the processor's memory is the only time the data is copied. The EPICS device support is written such that the waveform record's bptr field is just set to the memory location of the data. This makes the raw waveform viewable in a EDM XY graph widget for inspection, if desired. For LCLS operational frequencies of 30-120 Hz, the waveforms are only drawn at 0.5 Hz.

In the same loop (where the FIFO is read), the waveform of corrections is applied to the sample. The result is the processed waveform and the sum of the processed sample, in I and Q. If the channel needs to have its variance calculated, a second loop through the data is necessary.

At the end of the read, the processed values are available to the VME system to copy and use as inputs to feedback loops or for diagnostic displays.

PERFORMANCE

The SNR is better than 63dB on all four channels (Figure 7). If scaled to the ADC full scale this would be 69dBFS. The board may be able to achieve 79dBFS SNRs. There is also the possibility that the board layout and/or power supply connections contributes to this raised noise floor. Channel to Channel cross talk in all cases is lower than 100dB at 25.5MHz.

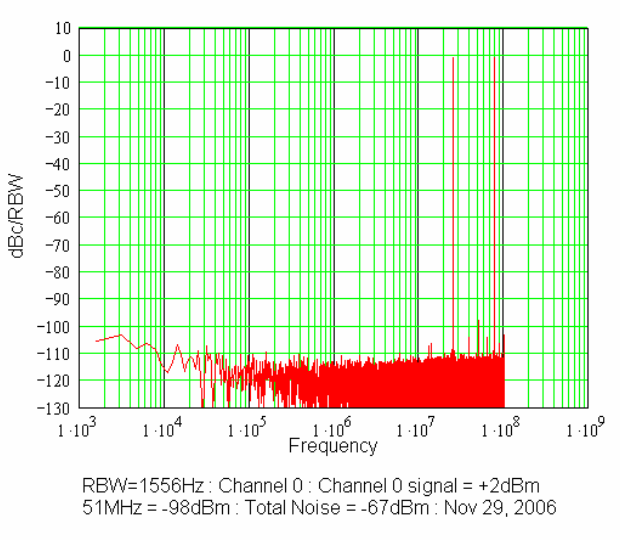

Figure 7: Channel 0 FFT with signal in channel 0