UPGRADE OF BPM DATA ACQUISITION SYSTEM USING REFLECTIVE MEMORY AT PLS

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Abstract

PLS(Pohang Light Source) is 2.5 Gev synchrotron radiation source in Pohang, Korea, which is under operation since 1995. The hardware and software of the old BPM(Beam Position Monitor) data acquisition system for the PLS storage ring was completely upgraded to increase its performance and stability. The new BPM data acquisition system is based on VME-based EPICS (Experimental Physics and Instrument Control System) IOC system. We used 16-bit resolution analog-to-digital conversion board to digitize analog BPM signals. We developed a data average software to average raw BPM data using reflective memory board. We also developed device drivers for VME I/O boards used, IOC database for PV's(Process Variables). The new BPM data acquisition system is currently running for routine operation with good performance and stability. In this paper, we present the hardware and software of the new BPM data acquisition system.

INTRODUCTION

The old BPM data acquisition system for the PLS storage ring was developed in 1995[1]. The old system consists of SCC (Subsystem Control Computer) for front-end processing and MIU(Machine Interface Unit) for direct interface to BPM. SCC and MU are both based on VME(Motorola 680x0) and OS-9 real-time operating system. MIL_1553B is used for the communication between SCC and MIU.

The hardware and software of the old system is very old and out of date. It has shown communication faults and system faults in unacceptable frequency. The old system doesn't have enough performance and stability to meet today's increased control requirements. So, we decided to completely replace the old system with up-to-date hardware and software with better performance and reliability. The upgrade of the old BPM data acquisition system is finished. Now the new system is under routine operation with satisfactory performance and stability.

The new BPM data acquisition system is based on VME-based EPICS IOC's. The new BPM IOC's also control corrector magnet power supplies for the storage ring. We developed data average software to average raw BPM data using reflective memory. CPU load of the new BPM IOC is measured above 50%. To reduce CPU load, we are going to separate BPM control and corrector magnet power supplies control function. We are also planning to develop a fast global orbit correction system using reflective memory in the near future. Figure 1 shows configuration diagram of the new BPM data acquisition system

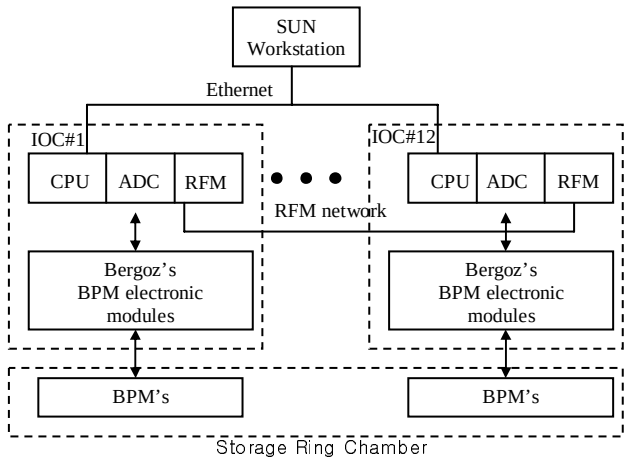

Figure 1: Configuration diagram of the new BPM data acquisition system

HARDWARE

PLS storage ring chamber has 12 cells and each cell has 9 BPM's. So, there are 106 BPM's in total in the PLS storage ring. We use Bergoz's electronic modules to pre-process beam position signals from BPM pick-up buttons in the chamber. The new BPM data acquisition system consists of 12 VME-based EPICS IOC's. There are 12 control sheds around the storage ring. In each control shed, there are one BPM IOC and 9 Bergoz's BPM electronic modules. At present, the BPM IOC not only controls BPM's but also controls corrector magnet power supplies in the storage ring. But, next year we are going to separate BPM control and corrector magnet power supply control function to reduce CPU load of BPM IOC.

Hardware modules in each IOC are SBC(Single Board Computer) board, ADC(Analog-to-Digital Conversion) board, and RFM(Reflective Memory) board. Motorola's MVME-5110 is used for SBC board. It has 500 Mhz PowerPC CPU chip and 128 Kbytes main memory. GeFanuc's VMIVME-3122 is used for ADC board. It has 32-channel inputs, 100Khz conversion rate, and 16-bit resolution. ADC board is used to digitize analog signals from Bergoz's electronic modules. GeFanuc's VMIVME-5565 is used for RFM board. This reflective memory board is fast, flexible and easy to use. Data is transferred by writing to reflective memory (SDRAM), which appears to reside globally in all RFM boards on the network. It has 2.12 Gbaud network transfer rate and 128 Kbytes reflective memory. RFM board is used to average raw BPM data from ADC board. Figure 2 shows picture of the new BPM IOC installed in the control shed. Table 1 shows list of hardware modules in the new BPM IOC.

Figure 2: Picture of the new BPM IOC.

Table 1: Hardware modules of the new BPM IOC

	Model	
CPU	MVME-5110	- MPC7450 PowerPC CPU chip - 512MB main memory
ADC	VMIVME-3122	- 16-bit resolution, - 100 KHz conversion rate
RFM	VMIVME-5565	- 128 MB reflective memory - 2.12 Gbaud network transfer rate

SOFTWARE

The software for the new BPM IOC consists of EPICS device support/driver for VME I/O boards, IOC database for PV(Process Varibles), and data average software. Figure 3 shows software structure of the new BPM IOC.

The new BPM IOC has two VME I/O boards: ADC(VMIVME-3122), RFM(VMIVME-5565). We developed EPICS device support/driver software for these boards.

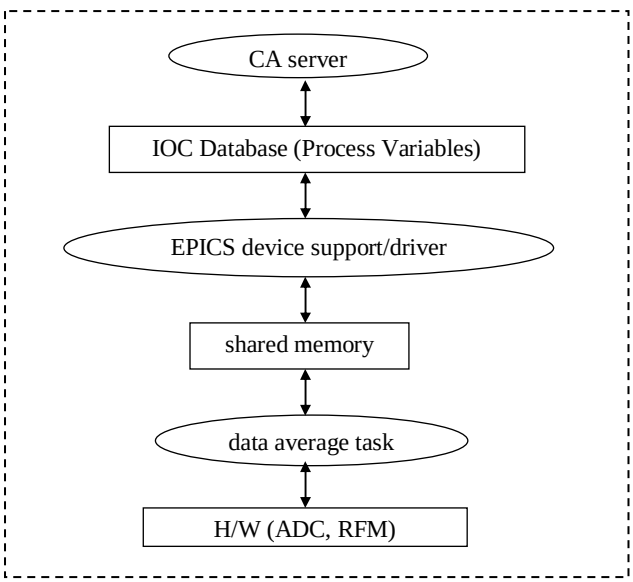

Figure 3: Software structure of the new BPM IOC.

There are 3 PV signals defined for each BPM: position_x, position_y, agc. So, There are 324 EPICS PV's in total for 108 BPM's in the storage ring. There are also tens of additional PV's for diagnostic purposes.

We developed a data average software to average raw data digitized by ADC board. The initial 2000 samples of raw data are stored into the reflective memory in sequence. Every time a new sample data is stored, the past 2000 samples are averaged and that is averaged BPM data. In this way, we could average 2000 samples of data in refresh rate 2 seconds. Data average software runs in independent task. We used shared memory technique to communicate between EPICS device support/driver and data averaging task. Figure 4 shows data average scheme used.

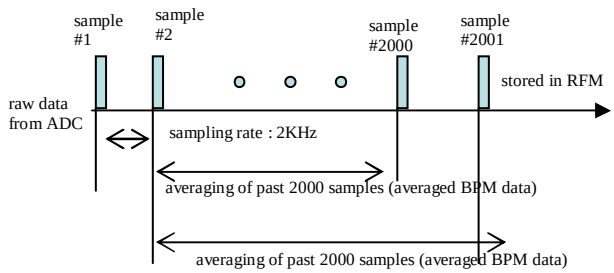

Figure 4: Data average scheme.

FUTURE UPGRADE PLAN

Our new BPM IOC controls not only BPM's but also corrector magnet power supplies. At present, CPU load of each BPM IOC is above 50%. We are going to separate BPM and corrector magnet power supply control function to reduce CPU load. We are also planning to develop a fast global orbit correction system utilizing reflective memory .

SUMMARY

We upgraded the old BPM data acquisition system of the PLS storage ring. The old system based on VME/OS-9 was replaced by VME-based EPICS system. We used 16-bit resolution ADC to digitize analog BPM signals. We developed data averaging software to average raw BPM data using reflective memory. We also developed EPICS device support/driver for the VME I/O boards used. We installed 12 new BPM IOC's in the control shed around the storage ring. Now the new BPM data acquisition system is under routine operation with good performance and stability.

REFERENCES

[1] I.S. Ko, J.W. Lee, J.C. Yoon, E.H. Lee, and B.R. Park, "Control System of PLS 2-GeV Storage Ring", ICALEPCS'97, Beijing, Nov 1997, p. 85.

[2] Martin R. Kraimer, APS, "EPICS Record Reference Manual".

[3] Martin R. Kraimer, APS, "EPICS Input/Output Controller Application Developer's Guide".