PLS FULLY DIGITAL CONTROLLED CORRECTOR POWER SUPPLIES

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ABSTRACT

As the beam-line users require more stringent beam stability for the advanced synchrotron experiments, fully digital controlled 20-bit magnet power supplies have been developed and successfully tested for closed orbit correction of Pohang Light Source (PLS). The new digital power supply has used fiber optics for 25 kHz switching of IGBT drivers and implemented DSP, ADC, Interlock, DCCT cards in a compact 3U-sized 19" chassis. Input-output low-pass filters suppress harmonics of 60Hz line frequency and switching frequency noise effectively. Overall performance of the power supplies has demonstrated ± 2 ppm short-term stability (< 1 min) and ± 15 ppm long-term stability (< 12 hours). All the existing 12-bit 70 power supplies for vertical correction magnets were successfully replaced with new digital power supplies during 2005 summer shutdown period (July 25 ~ September 10).
In this paper, we will describe the hardware structure and control method of the digital power supply and the test results will be shown.

INTRODUCTION

Pohang Light Source (PLS) is a 2.5 GeV third generation synchrotron light source located at Pohang, Korea. The storage ring (SR) of PLS has installed 70 horizontal and 70 vertical type correction magnets power supplies (PS). PLS has successfully installed and commissioned newly upgraded fully digital controlled 70 vertical corrector power supplies during 2005 summer shutdown period (July 25 ~ September 10). Storage ring PSs are requiring of very high output current performance for keeping the tune and orbit very stable. Important PS considerations include reproducibility, long-term and short-term stability and resolution. Already some other facility has developed highly stable PS to increase orbit stability and development of new power electronics technology [1].
In recent years, accelerator power supply technologies evolved from traditional analogue topology to digital topology because of this digital technology have many advantages and can improve machine flexibility.

PLS commissioning started in 1994, and the beam has been served to users since September of 1995. As the construction of 6 insertion device (ID) beam line completed, users require more stable photon beam. The SR global orbit feedback is required to keep sub-micron order orbit stability. Third generation SR correction power supplies (CPS) must satisfy high confidence, stability (± 15 ppm) and resolution (> 19-bit, 2 ppm).
Especially for fast control with single board computer (SBC) such as VME, reproducibility, stability and resolution are very important for implementation to sub-micron orbit stability.
Since the first stage (1994) PLS CPS has chosen 12-bit reference digital to analogue converter (DAC) and hysteresis current control methods without any output filters, switching harmonics are directly modulated to magnet field. 12-bit CPS has a biggest problem that 1-bit minimum kick value is 54 mA (maximum current is ± 110 A) that makes a lot of orbit fluctuation (1.0 μrad), Second stage upgrade to 16-bit DAC is 3.35 mA per bit (0.06 μrad). In the third stage (2003), 24-bit DAC card was chosen from BESSY-II[3] and 22 straight section PS's were replaced. In 2004, PLS made decision to develop new digital controlled CPS same as PSI digital technology [2].

PLS has developed new correction PS that adopted full digital controlled technology according to requires of orbit feedback specifications listed in Table 1. It is developed in collaboration with PSI (Paul Scherrer Institut) EE group and DLS (Diamond Light Source) EE group.
New developed CPS has used full digital technology and fast communication with SBC, control of current regulation loop and managements of analogue and digital signals, which are dc voltage, current

and status. The power supplies operate at 25 kHz PWM switching frequency and are rated for ± 110 Amps, ± 11 Volts, 2 ppm step resolution, 2 ppm shorter stability and ± 15 ppm long-term stabilities with vertical magnet loads.

In this paper, the PLS new CPS hardware and controller structure, experimental results and commissioning results are presented.

HARDWARE CONFIGURATION

H-Bridge four-quadrant power converter

Proposed details hardware block diagram of the four-quadrant CPSs is shown Figure 1 (a). The full-bridge structure IGBT switch state is on and off by 25 kHz unipolar PWM Patten, (+)(-) current throws to magnet load. The power module is IGBT (600 V / 300 A EUPEC), DCCT is Danfysik ULTRASTAB-867 and burden register is VHP-4 type ± 5ppm/°C at 45 Ω from VISHAY. Output filter is 5th LC network and parallel damping capacitor cut-off frequency is 4.5 kHz. Fiber optics for 25 kHz pulse width modulation (PWM) signals delivered to IGBTs, a driver that used low cost EXB841 from Fuji Company. DC-link voltage and output voltage are divided by voltage sensing module and connected to ADC input channels. DC-link voltage is used to feed-forward feedback signals, output voltages calculates load resistance and monitoring. DCCT output voltages (110 A / 5 V) for current measurement are directly connected with parallel four-channels ADC input for 1st order low-pass filter and over-sampling (200 kHz) that has achieved over 18-bit resolutions. Regulation loops are two types: first is voltage feed-forward for fast compensation DC-link voltage variations, second are proportional-integral (PI) with anti-windup for output current regulation that is used to guarantee null steady-state error with rise times of step response. More details of diagram are shown in Figure 1 (b).

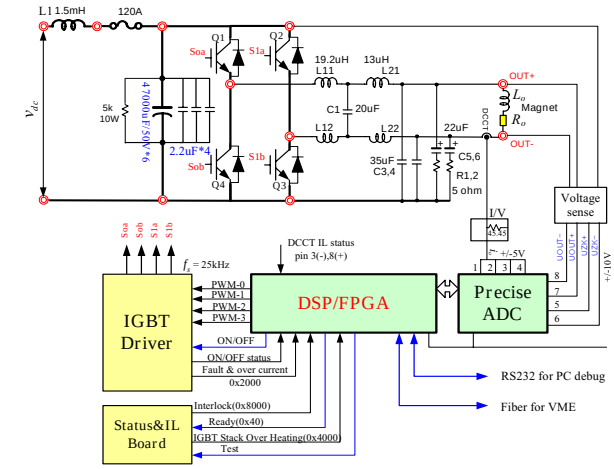


Figure 1: Block diagram of the proposed hardware:

(a) Power circuit diagram (b) the regulation loops block diagram

Hardware specification

Table 1 illustrates the PLS vertical correction PS specifications. Digital PS is achieved output current with resolution equivalent over 19-bit and stability is ± 15 ppm with digital control loops. The

switching frequency depends on power semiconductor such as FET or IGBT. For our case, fast IGBTs used for low cost high reliability and operation frequency is 25 kHz at ± 110 Amps with LC filters.

Parameters	Specifications
Output voltage/current	± 11 V, ± 110 A
Load inductance	16 mH @1 kHz
Operating quadrant	4 Q
Stability (0 sec to 60 sec)	± 2.5 ppm
Stability (> 12 hours)	± 10 ppm
Resolution of output current	> 19 bit
Reproducibility	± 5 ppm
Filter cut-off frequency	4.5 kHz
Switching frequency	25 kHz PWM

Table 1: The specifications of correction PS

DIGITAL CONTROLLER

Figure 2 shows 3U size DSP and AD/DA cards for implementation of digital control power supplies. The core processor is Analog Device SHARC ADSP-21065L 66 MIPS floating-point capabilities with 66 MHz clock. FPGA used for PWM generation and communication with 5 Mbps fiber channels and 115.2 Kbps serial as well as 16 digital inputs, 8 digital outputs. For the accelerator control system, 5 Mbaud applied with VME SBS for fast global control system as well as service mode support serial port (RS232) that is very easily testing and diagnostics. DSP internal tasks are running every $20\mu s$ (25 kHz PWM frequency) for regulation of loops which perform calculation of error compensation and communication with AD/DA cards.

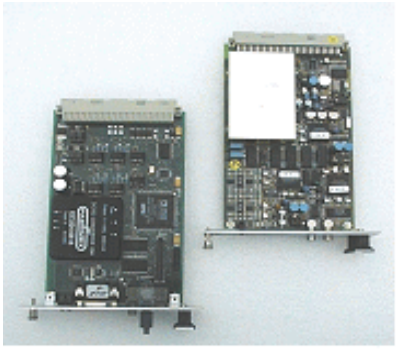


Figure 2: Digital control cards from DIAMOND

Left: DSP card, right: ADC card

EXPERIMENTAL RESULT

Experimental Result

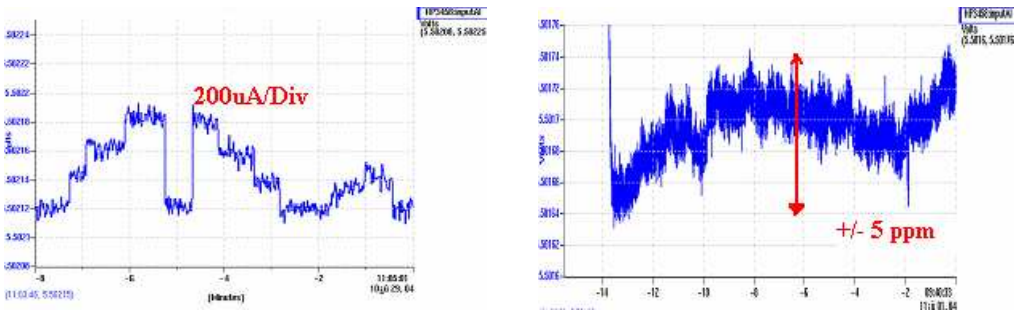
Figure 3 shows completed product of new digital controlled CPS in PLS storage ring. The four-quadrant converter is designed as a 4U module located in a 19” rack. Power stack is covered with 2 mm flat copper and cooling water is low conductivity water (LCW) 25 °C. The measured points were

output step resolution, long-term stability and frequency characteristics that are important factors for determining PS performances. For the measurements of performance, HP3458A $8 \cdot 1/2$ digit digital multi-meter (DVM) from Agilent and SR780 dynamic analyzer from Stanford Company were used.

Figure 3: Completed of Digital PS

Current Stability

Figure 4(a) has shown step response characteristics for 100 μA step reference and also (b) is 12 hours stability at 55 Amps output current that is keeping $\pm$ 5 ppm during 12 hours.



(a) (b)

Figure 4: Output current measurement: (a) Step response at 55 Amps (200 μA /Div)

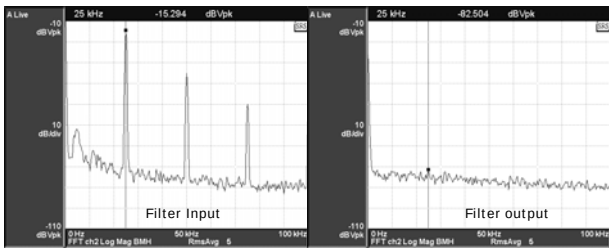
(b) Long term stability at 55 Amps (13 hours, 200 μA /Div)

Output Filter

The output filter requires very low high-frequency noise ripple on the output. We designed 5th order low pass filter with parallel damp filter, which is very common approach to design.

Figure 5 shows output filter characteristics at 25 Amps, (a) is frequency spectrum before filter. This centre frequency is same as switching frequency 25 kHz, 2nd and 3rd harmonics are also modulated. (b) Has shown frequency spectrum after filtering.

According to this measured result of spectrum characteristic the most switching frequency 25 kHz and its harmonics were attenuated about –90 dB.



(a) (b)

Figure 5: Filter frequency response @ 25 Amps:

(a) Before filtering (25 kHz, 50 kHz and 75 kHz) (b) After filtering

Subsection Headings

Figure 6 shows output currents of digital controlled vertical CPSs in operation. The biggest current is in ID sections such as U7, U10 and EPU6.

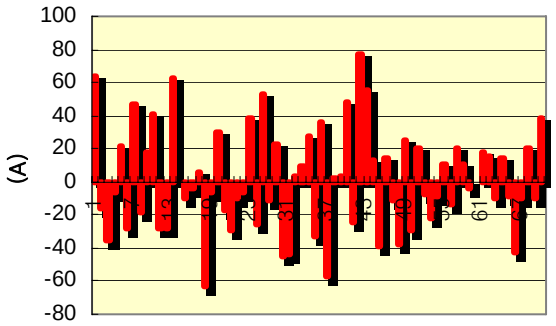


Figure 6: Operating output currents of vertical corrector

CONCLUSION

PLS successfully replaced and realized commissioning of high performance digital controlled power supplies to PLS storage ring. It was possible for the second time to use digital controller with real beam. It has clearly solved problems of old PSs: resolution, stability and high frequency noise. The operation result was very satisfied with fast control response, high resolution and accuracy. DSP, FPGA and ADC based digital control algorithm is capable over 19-bit resolution and ± 15 ppm stability. Also we designed 4.5 kHz cut-off frequency output filters for attenuation of switching harmonic with –90 dB attenuations. At present 70 corrector power supplies are in operation at the PLS storage ring for global orbit feedback operations and the performance is very excellent.

ACKNOWLEDGEMENT

This work is supported by Ministry of Science and Technology, Korea. The authors gratefully thank to F. Jene, L. Tener in PSI and T. Dobbing in DIAMOND for the advice and support during the work.

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