DATA ACQUISITION FOR SNS BEAM LOSS MONITOR SYSTEM

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Abstract

The Spallation Neutron Source (SNS) beam loss monitor system uses VME based electronics to measure the radiation produced by lost beam. Beam loss signals from cylindrical argon-filled ion chambers and neutron detectors will be conditioned in analog front-end (AFE) circuitry. These signals will be digitized and further processed in a dedicated VME crate. Fast beam inhibit and low-level, long-term loss warnings will be generated to provide machine protection. The fast loss data will have a bandwidth of 35kHz. While the low level, long-term loss data will have much higher sensitivity. This is further complicated by the 3 decade range of intensity as the Ring accumulates beam. Therefore a bandwidth of 100kHz and dynamic range larger than 21 bits data acquisition system will be required for this purpose. Based on the evaluation of several commercial ADC modules in preliminary design phase, a 24 bits Sigma-Delta data acquisition VME bus card was chosen as the SNS BLM digitizer. An associated vxWorks driver and EPICS device support module also have been developed at BNL. Simulating test results showed this system is fully qualified for both fast loss and low-level, long-term loss application. The first prototype including data acquisition hardware setup and EPICS software (running database and OPI clients) will be used in SNS Drift Tube Linac (DTL) system commissioning.

INTRODUCTION

The Spallation Neutron Source facility, which is being built at Oak Ridge National Laboratory (ORNL) by a partnership of six Department of Energy (DOE) laboratories [1], is designed to accumulate 1.5 x 10^{14} protons at 1.0 GeV and deliver them to the experimental target in one bunch at 60Hz. The 1.4MW beam power produced by average current of 1.4mA at target makes it crucial that losses be kept extremely low to allow normal accelerator maintenance without high background radiation [2]. Therefore a Beam Loss Monitor (BLM) system has to be employed to minimize the uncontrolled beam losses by providing data for tuning machine and by inhibiting the beam when excessive losses occur.

Based on the experiences achieved from the Relativistic Heavy Ion Collider (RHIC) operation, Brookhaven National Laboratory (BNL) designed a BLM system to measure beam losses from a maximum 1% local loss down to a 1 W/m operating loss tolerance. Resolution of 1% of the 1 W/m threshold also has been requested. This amounts to a dynamic range of about 2 x 10^{6} for the system, which would require at least 21 bits digitizing range [3]. Cylindrical argon-filled ion chambers, similar to those proven in RHIC operation, will be used as the primary detectors. More sensitive neutron detectors will be installed in the lower energy portions of the linac to capture the loss signals at lower energy.

HARDWARE

In order to meet the above requirements, a VME bus prototype of BLM Input/Output Controller (IOC) consisting of commercial processor module, digital I/O module, analog I/O modules, High Voltage Power Supply (HVPS) module, custom designed timing modules and signal condition module has been built at BNL.

System diagram

A schematic diagram of a minimum configuration BLM IOC is shown in Figure 1.

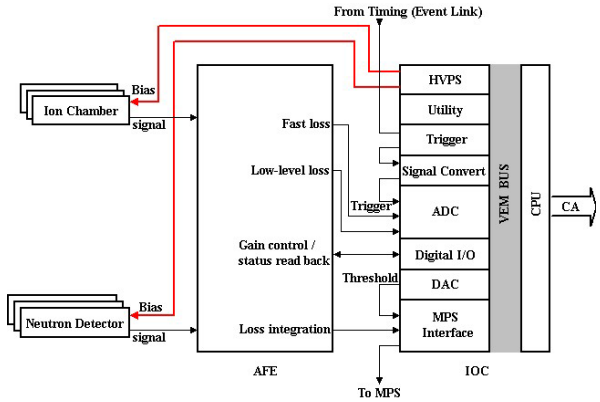

Figure1: SNS BLM data acquisition system.

Ion chambers and neutron detectors, which are powered by HPVS, will produce output current signals when beam losses occur. These signals are split 3 ways and converted to voltage signals in AFE module. One path is integrated to the Machine Protection System (MPS) signal sensing circuit, one to the fast output for wideband monitoring and one for the low-level 1 W/m monitoring. Then these conditioned voltage signals are fed into dedicated BLM IOCs and further processed to provide data to document the beam loss distribution and provide signals to inhibit the beam.

The prototype BLM IOC with minimal configuration includes the following modules. MVME2100 running EPICS iocCore and device support modules provides controls for others I/O modules and data services for high-level applications. Custom designed SNS utility module collects chassis environment information and provides an interface to the SNS event and real time data link system. The beam synchronous trigger module (V124S), modified from RHIC's version, monitors the SNS event link and responds to a predefined event to produce a trigger signal, which determines the start time

of data acquisition. The signal condition module (V294) also is custom designed by BNL and converts V124S standard TTL output signal to digitizer wanted differential TTL signal and enlarge pulse width (trigger gate window) to 4ms, which is required by BLM data process. A 32 channel, 24 bits and 100kHz sample rate ADC module, ICS110BL is adopted as BLM digitizer to acquire both fast loss and low-level, long-term loss data. A flexible digital I/O card (VMIC2510B) is used to set fast channel programmable viewing gain and read back serial number and jumpers setting of AFE module. A 12 bits IP DAC module (HyTec8402) attached on IP carrier (VIPC618) provides threshold of beam inhibit based on user setting value. The custom designed MPS interface card compares beam loss integration output with user setting threshold to produce an inhibit signal in the event of excessive loss. VME bus controlled 2 channel HVPS modules (ISEG204L) is used to provide bias high voltage to ion chambers and neutron detectors.

Digitizer

Successful operation of BLM system is dependent upon the accuracy and reliability of the digitizer. The fast loss data process requires the digitizer to have high bandwidth and large onboard memory. While the low-level, long-term loss data has much higher sensitivity but only requires a few Hz bandwidth. Summary of both of their requirements for digitizer are shown in table 1.

Table 1: BLM digitizer requirements

Bandwidth	>= 35kHz
Sampling Rate	>= 100kHz
Arming Rate	>= 60Hz
Memory Size	>= 400 samples / channel
Averaging Deviation	<= 20μV

In order to select a qualified digitizer from available commercial cards we built a Labview, ActiveX CA clients and EPICS based ADC module evaluation environment. Factors such as linearity, deviation, thermal drift and so on were measured for several types of VME digitizer modules. Based on the test results the 32 channel, 24 bits high throughput VME bus sigma-delta ADC module (ICS110BL) was adopted as BLM digitizer, which can provide much better performance with a little bit higher cost per channel [4].

SOFTWARE

BLM is a part of SNS control system, which is developed using EPICS tools kit. Shared resource and collaboration of EPICS reduces a lot of software development work for I/O modules (such as HyTech8402 DAC module and ISEG204L HVPS module) used in BLM IOC. Meanwhile the software for the utility module and beam synchronous trigger module has been done by SNS. So the main task of BLM software development is writing an efficient driver for ICS110BL digitizer to support up to 60Hz update rate and 3.8 Mbytes/s data throughout rate.

Figure 2 shows the block diagram of digitizer software, which can be divided into two main parts: vxWorks support module and EPICS device support module.

ICS110BL vxWorks support module includes a Virtual Digitizer (VD) data structure, an ICS110BL Interrupt Service Routine (ISR), a DMA controller driver, a DMA ISR, a Hardware User Interface (HUI) and a Virtual Digitizer User Interface (VDUI). Before IOC initialization VD will be registered and created in local memory to map all parameters and data acquired by real digitizer. After that the IOC initializing routine will configure and start digitizer with parameters stored in VD. While data acquisition done ICS110BL will generate a VME bus interrupt to indicate acquired data ready.

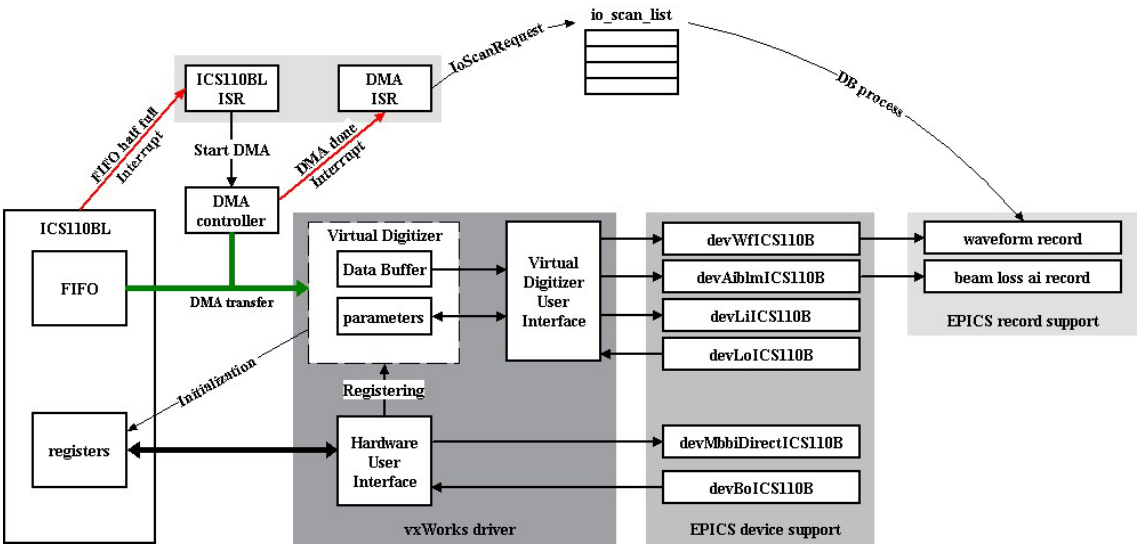

Figure2: Block diagram of digitizer software.

ICS110BL ISR configures MVME2100 onboard DMA controller to start a DMA transfer to move data from digitizer FIFO to local memory buffer resides in VD. When DMA transfer is done the controller will generate another VME bus interrupt to indicate VD data ready. Then user can read back mapped data through VDUI instead of accessing digitizer FIFO via VME bus directly. This architecture isolates user random read access from VME bus read access and guarantees user always getting the newest data.

Six EPICS device support modules are designed for ICS110BL digitizer and BLM application:

- devWfICS110B. Call VDUI routines to read back raw waveform data of beam loss signal.
- devAiblmICS110B. Dedicated ai device support module for SNS BLM application. Call VDUI routines to read back raw data and calculate baseline adjusted integration value of loss pulse.
- devLiICS110B. Call VDUI routines to return parameters of registered digitizer such as sampling rate, trigger rate, buffer size and so on.
- devLoICS110B. Call VDUI routines to set new value of digitizer parameters such as sampling rate, buffer size and so on.
- devMbbiDirectICS110B. Expert interface used for digitizer debugging and maintenance. Call HUI routines to monitor digitizer registers such as control register, status register and interrupt vector register.
- devBoICS110B. Expert interface used for digitizer debugging and maintenance. Call HUI routines to set individual bit of digitizer control register.

APPLICATION

The first prototype BLM data acquisition system including EPICS running database and EDM control panels has been implemented at ORNL for SNS DTL commissioning. A total of 9 ion chambers and 3 neutron detectors are employed to acquire beam loss signals.

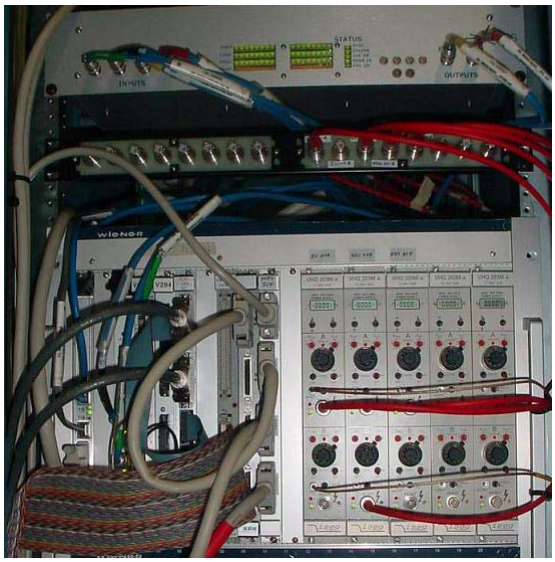

Figure3: BLM prototype for SNS DTL

Figure 3 shows the front panel of MPS chassis and BLM IOC, which has minimal configuration plus four more HVPS modules. One HVPS is used to provide bias voltage for ion chambers chain, another two are used to provide bias voltage for neutron detectors, and the others are reserved for more detectors.

Actual beam loss signals have been acquired from neutron detectors during August 2003 commissioning (Fig. 4). With 200MHz MVME2100 card, single digitizer and 30Hz data rate we can get about 40% usage of CPU loading. So double digitizers and 60Hz data rate is hard to supported with this prototype. More powerful CPU modules such as the MVME5100 must be considered for use in other subsystems.

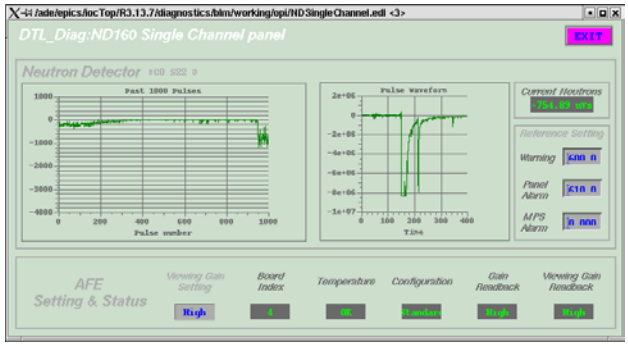

Figure4: Actual signal captured from neutron detector.

SUMMARY

During the past two years the SNS BLM data acquisition system has been designed and developed by BNL. Simulating beam tests at BNL and captured actual beam loss signals at ORNL shows this system can meet both single pulse loss monitor and 1W/m long-term, low-level loss monitor requirements. More test and improvements such as better human interface, new data process method implementation, system performance evaluation and so on will be done in the future DTL commissioning. This system will be duplicated to CCL, HEBT, Ring and RTBT subsystems.

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REFERENCES

[1] http://www.sns.gov/partnerlabs/partners.htm
[2] http://www.sns.gov/aboutsns/baseline.htm
[3] http://www.sns.bnl.gov/sns_icd_doc.asp
[4] Y. Leng, L. Hoff, “ADC Module Evaluation Report for BLM System”, BNL Non-published report, July 2002.