J-PARC TIMING SYSTEM

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Abstract

We present the design and the configuration of the timing system for Japan Proton Accelerator Research Complex (J-PARC, formerly known as JKJ). J-PARC consists of a 400-MeV linac, a 3-GeV rapid cycling synchrotron (RCS) and a 50-GeV synchrotron (MR), those different repetition rates are 50-Hz, 25-Hz and 1/3.64-Hz, respectively. In each pulse, the linac and the RCS have the different destinations of the beam as follows; the linac is operated for the RCS and the accelerator-driven nuclear transmutation (ADS) alternatively. In the case of the RCS, four pulses in the 91 pulses in the MR cycle are for the MR injection and the others for the 3-GeV beam users. Hence, the linac and the RCS are required to be operated in different modes and timing in each pulse. To realize this operation, a control word, so-called "type", is sent from the central timing control before each 50-Hz trigger. The "type" presents the operation type of the accelerator during the next 50-Hz period. Each receiver module for each target device in the power-supply rooms sets the delay-value from look-up table (LUT) according to the type information. The whole timing system is based on the master clock generated by a high-stability synthesizer. The master clock is chosen to be 12-MHz. The 50-Hz trigger clock is generated by counting the master clock. We also describe the prototype timing modules.

INTRODUCTION

Japan Proton Accelerator Research Complex (J-PARC) is a project of a high-intensity accelerator complex which consists of a 400-MeV linac, a 3-GeV rapid cycling synchrotron (RCS), and a 50-GeV synchrotron (MR). Since the intensity of the accelerating beam is high, the beam loss must be limited as small as possible to avoid the activation of the accelerator devices. The precise beam control is required and hence the stable timing / trigger system is necessary. The jitter of the trigger must be below 1-nsec.

We define two kinds of timing, *scheduled timing* and *synchronization timing*. The scheduled timing is defined by a delay determined in advance from the 50-Hz *trigger clock* sent from the central timing control. Most devices and power supplies run with the scheduled timing. The synchronization timing is based on the trigger generated by the accelerator devices other than the central timing control. For example, the extraction kicker of the RCS fires based on the trigger from the RF system to be synchronized with the real circulating beams. In this article we focus on the scheduled timing system.

The linac, RCS and MR are operated at the different repetition rate of 50-Hz, 25-Hz and 1/3.64-Hz, respectively. The linac and the RCS have different beam destinations in each pulse as follows. (1) The linac is operated for the RCS and the accelerator-driven nuclear transmutation (ADS) alternatively. (2) Four beam pulses in the 91 pulses of the RCS (25-Hz repetition) in the MR cycle are lead to the MR and the others are for the 3-GeV beam users. Hence, the linac and the RCS must be operated in the different modes and the different timing in each pulse. The beam destinations are scheduled. The realization of the operation is described in Section . We also describe the prototype modules and their performance.

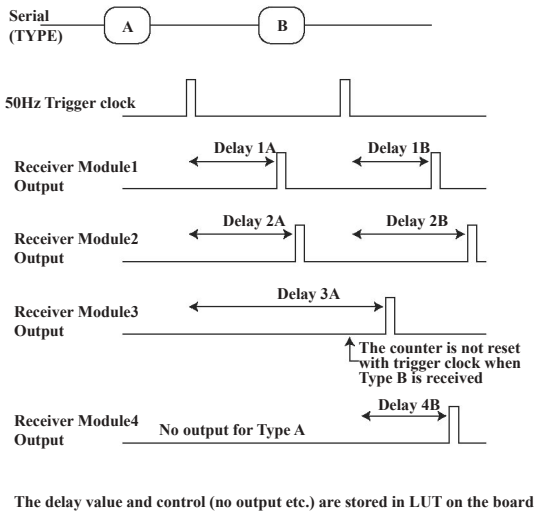

Figure 1: Operation principle of the scheduled timing system

CONFIGURATION OF THE TIMING SYSTEM

Operation principle

Figure 1 shows the operation principle of the scheduled timing. As described in the previous section, the scheduled timing is defined by a delay from the 50-Hz trigger clock sent from the central timing control to the facilities. Before the trigger clock is sent timing-control, a control word (so-called "type" which presents the operation type of the accelerator during the next 50-Hz period) is broadcasted to the receiver-modules for the target devices in the power supply rooms. Each receiver module has own memory which determines the behavior during the next period according to the type information. Three behaviors are defined, (1) to output a trigger pulse at a proper delay, (2) to suppress pulse output during the next period, and (3) to continue the delay-counting beyond the trigger clock. By this way, the target devices can run at the different timings

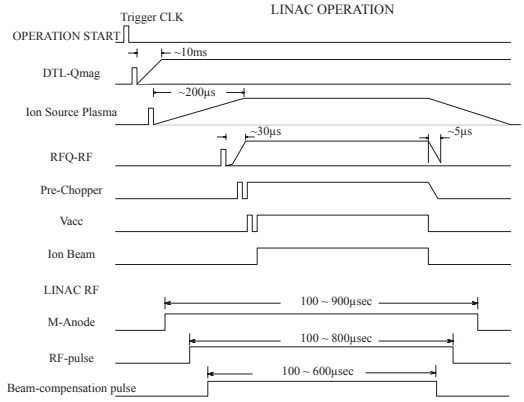

Figure 2: Linac timing chart

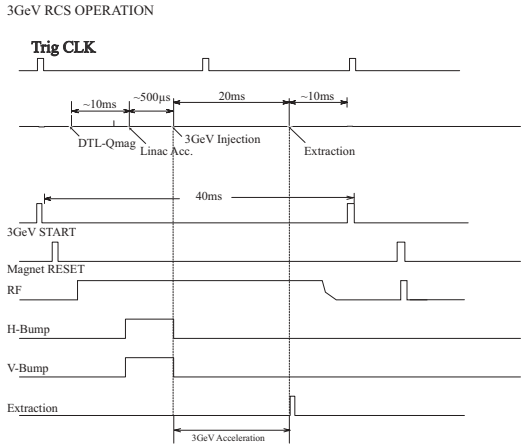

Figure 3: RCS timing chart

to realize the different mode every 50-Hz period.

Since the power supplies for the lattice magnets of the RCS and MR are operated independently from the AC line frequency, the timing system does not need to synchronize with the AC line frequency. The whole timing system is based on the master clock generated by a high-stability synthesizer. The clock is chosen to be 12-MHz, by which the linac accelerating frequency 324-MHz can be divided. Also, the 50-Hz trigger clock is generated by counting the master clock.

Timing chart of each accelerator

There are 91 RCS cycles in a MR cycle (50-GeV MR normal operation). Timing of main components of the linac is shown in Figure 2. The power supplies of the DTL-Q have the rise time of about 10 msec and are triggered first. Output beams from the linac are injected into the 3-GeV RCS. The timing chart of the RCS from injection to extraction is shown in Figure 3. The MR has fast and slow extraction modes. Time marks from P0 (=P5) to P4 shown in Figure 4 indicate start of MR injection, start of MR acceleration, end of MR acceleration and MR deceleration for the next cycle, respectively.

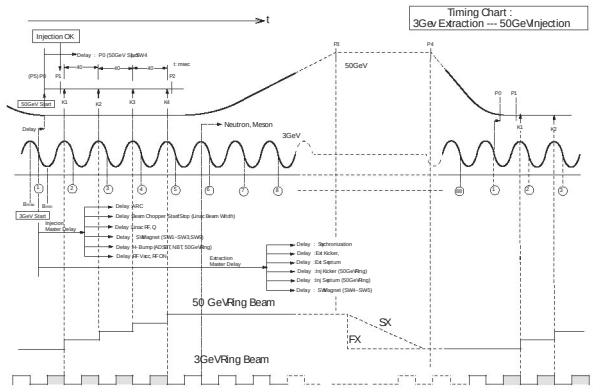

Figure 4: MR timing chart

Hardwares

In the central timing control, the following modules and devices are installed. A high-stability synthesizer is the reference of the clock generator, which outputs the 12-MHz master clock. The 50-Hz trigger clock is generated by the trigger clock generator counting the master clock. The timing control transmitter sends the “type” information every 50-Hz period. The type is sent after it is serialized. For the distribution of these three signals, the master clock, the trigger clock and the type, to the facilities in the J-PARC, the fanout and the E/O modules are used.

The three signals are sent via optical fibers from central timing control. A set of O/E, fanout and E/O modules are used for dividing the signals at the relay-station in each facility, if necessary. This is a star configuration and all facilities receive the same signal / information (clock, trigger clock and type).

A schematic of the timing panel in the power supply room is illustrated in Figure 5. In the power supply room in the accelerator facilities, the three signals are converted to electric signal by the O/E modules and then led to the timing control receiver modules. The receiver module is key component which generates the trigger pulses. The de-

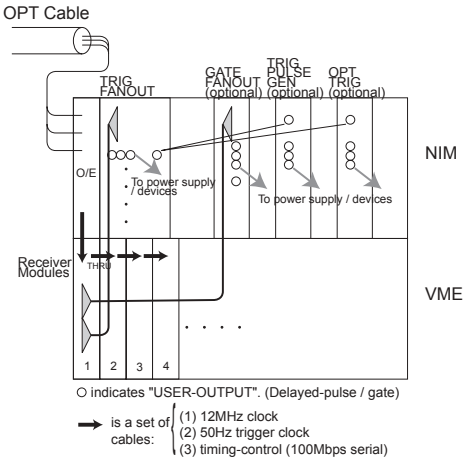

Figure 5: Timing receiver panel

tails of the module are presented in the next section. The 8-ch output pulses are led to the trigger fanout and gate fanout modules, which convert the signal level required by the power supply. Optionally, the trigger pulse generator, which converts the pulse width, and the E/O converter module are used according to the request of the power supplies and the devices.

Timing control transmitter and receiver

The transmitter module has the type-memory, which stores the sequence of the type word. The transmitter sends the type one-by-one from the type-memory with every trigger clock. The length of the sequence is arbitrary and the sequence ends with the end-word. The maximum length of the type-sequence is 1024. One type-sequence corresponds to one MR cycle. A special word "S" is sent at the beginning of a MR cycle. The word width of the type and "S" is 32-bit. They are sent after serialized. The word consists of four subsections, "A" (7-bit), "B", "C" and "D" (8-bit). The MSB of the word represents "S". The receiver module has a DIP switch to determine which subsection is used as the type for the module.

The receiver module has a look-up table (LUT), which contains delay words (delay value and control bits). The delay words are downloaded into LUT. The receiver picks up the delay word from the LUT according to the received type. Upon receiving the trigger clock, the receiver module starts an internal delay counter and outputs a delayed-pulse on the scheduled delay timing. The delay word width is to be 24-bit and the delay counter runs at the clock of 96-MHz, which is generated from the 12-MHz master clock by a PLL. Hence, the module can count up to 170 msec. By the control bits in the word picked up from the LUT, the counter in each channel works as one of the following ways. (1) The counter is reset by the trigger clock and starts counting until the delay value and then output a pulse. (2) During next period, the channel does not output a pulse. (3) The counter continues the counting without reset when the trigger clock comes, and outputs a pulse at the specified delay value. This feature is necessary for the timing of the RCS and MR, which runs at the repetition rates of other than 50-Hz. (4) Also, VME interrupts can be generated by setting of one of the control bits.

The receiver module has a set of through ports for cascading the additional receiver modules. It has 8 independent channels. The important outputs of the receiver module are listed below. The delayed-pulse and/or the Gate-out outputs are sent to the driver modules.

- Delayed pulse out: 8-ch independent output. These work in the manner described above.
- Gate out: 4-ch. This is set by the one of the delayed-pulse channel and reset by the other.
- Type out: The received type is stored in the register in the module and output from the front panel.
- Trigger count: This output shows the number of trigger clock after the start of the MR cycle.

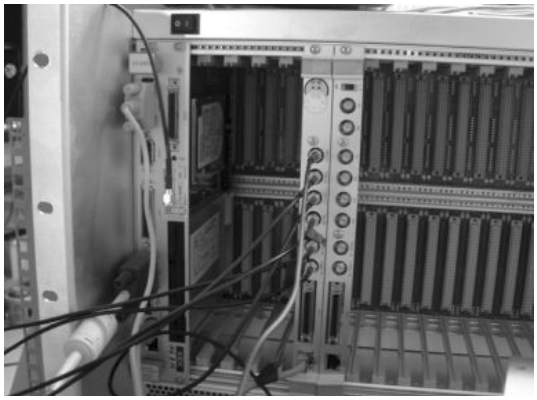

Figure 6: Prototype modules

PROTOTYPE MODULES

The prototype modules have been built and tested. We built the clock generator module, the trigger clock generator, the timing control transmitter and receiver modules. The receiver module has four output channel and the output pulse voltage is 3.3V. The operation principle is the same as the current design. A picture of the modules is shown in Figure 6.

The test was performed with a high-stability synthesizer (Agilent 8247C). The jitters of the clock generator and the trigger clock generator was below 50-psec (FWHM). By the combination of the timing control transmitter and receiver module, the overall jitter is around 500-psec. The test result meets the requirements.

SUMMARY

- J-PARC works based on the two kinds of timing, *scheduled timing* and *synchronization timing*.
- The scheduled timing system, which realizes the different operations every 50-Hz period, has been designed and considered. This system fits the requirements to run the three accelerators (linac, RCS, MR) which have the different repetition rates.
- Prototype modules have been designed and built. The output jitter of the prototype modules meets the requirements of J-PARC.

ACKNOWLEDGMENT

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