

NEW FEATURES OF THE SLS TIMING SYSTEM

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Abstract

The timing system of the Swiss Light Source (SLS) is based on the global event distribution, which has been running successfully over the last two years. To fulfil the ongoing demands of different subsystems and beamlines the timing system has been upgraded and introduces some new advanced features, which, adds more flexibility and more simplicity in terms of system implementation. The new version of the event generators (EVG) are equipped with the 500 MHz input (as external clock reference) and 50 Hz AC input (main supply). Therefore the synchronization to the main RF and AC main supply is done inside the EVG card without using any other hardware. The other nice feature of the new version is so called multiplexed counters whose outputs can be used in different ways to produce timing signals. One of the latest applications of the upgraded timings is to provide required synchronization to the FEMTO experiment in Surfaces / Interface Microscopy (SIM) beamline. The existing controls software (EPICS record and device supports) has been modified to support all the new features. The new hardware capabilities and their applications are explained in this paper.

GLOBAL EVENT SYSTEM

The Swiss Light Source is using so called global event system for timing of its facility. As shown (Figure 1) it normally comprises one event generator (EVG) and many event receivers (EVR). The system was first developed at the APS and then redesigned for the SLS.

The timing signals which have to be available to other subsystems or needed for synchronisation of the accelerator components and beam lines are applied to the EVG, example of these signals are main RF, main AC (50 Hz), ramping clock etc. Then all timing information (hardware or programmed by software) are converted to eight bit wide event codes and are transmitted at 50 Mbytes/sec via fibre optic links running at the speed of 100 Mbytes/sec to the all event receivers. The remaining 50 Mbytes/sec is used as a distributed bus sending status of 8 bus signals sampled at 50 MHz. There are eight TTL level inputs each will be assigned an event code to be transmitted. There are two 512 Kbytes sequence RAMs each can be enabled at a time independently to transmit its contents upon an external trigger (start sequence). The RAM contents are in fact programmed events with certain delays depending on their position in the sequence RAM. In most of the accelerator complexes there are situations that a sequence of actions has to be done at certain times respectively. The sequence RAM is used at such a situation (e.g. gun trigger, firing of the pulsed magnets for injection to booster, start of RF (and magnets) ramp etc.).

Event receivers can respond to the incoming event codes in different ways as well as recovering the status of the signals on the distributed bus. An EVR doesn't care if the event is in the sequence RAM or assigned to an external signal. It just reacts to the received event code in a way it has been programmed to.

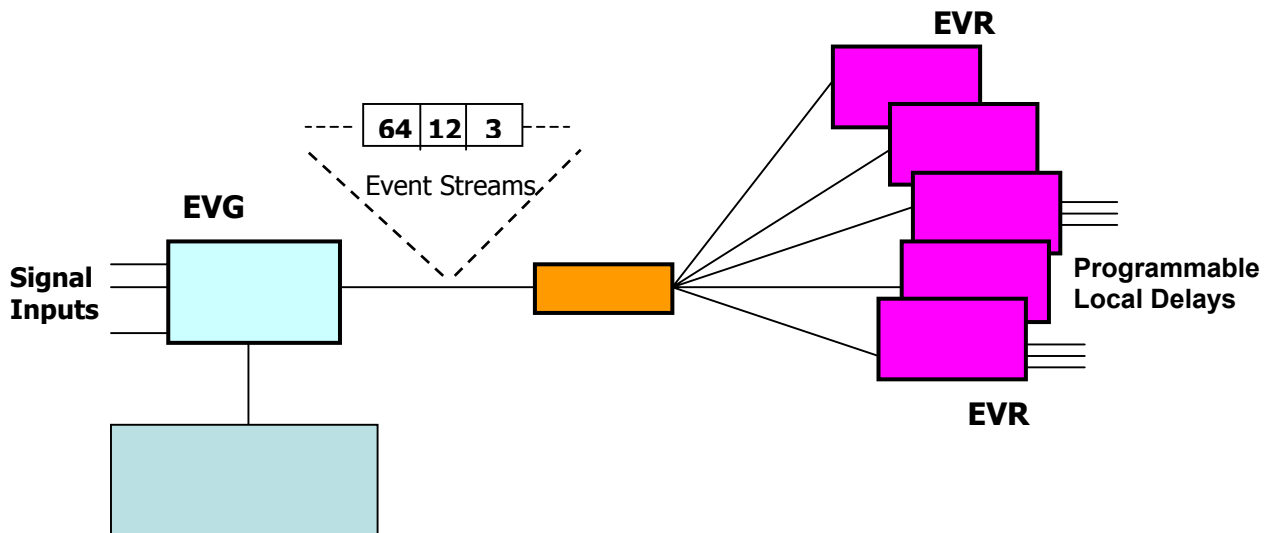


Figure 1: Global event system architecture.

NEW FEATURES

Not all the features of the event system (like interrupts, and time stamp counters) that are in use at the SLS have been explained so far. Here we just want to emphasize on new functionalities added to the event system. These features have affected whole the system but practically are results of hardware and FPGA/Firmware design modifications on the EVG card.

AC and 500 MHz Inputs

The latest version of the EVG (EVG-110 plus) has been equipped with a direct input for 500 MHz (main RF frequency) signal as an external clock reference. The advantage is to eliminate any down conversion unit in between, bringing up the precision of the system clock phase-locked to the main RF frequency of the accelerator.

A 50 Hz 3-12 VAC signal can be applied to the front panel of the EVG card. This signal can be down converted by a programmable eight-bit counter to required frequency (e.g. repetition rate for injection) and may be synchronized to a clock derived from the reference clock (500 MHz). This synchronised signal can then be used to trigger any of the sequence RAMs or an external event. All these are done by only proper setting of the registers or control bits of the EVG, which are well mapped to the VME memory.

Multiplexed Counters

Multiplexed counters are other nice feature of the new EVG design. There are eight 16-bits counters each can be reset by external signal or by register access via VME bus. As shown in Figure 2, output of each toggle flip-flop may be sent independently (multiplexed) to trigger external event inputs or as a signal on the distributed bus. This output can also be used to trigger the sequence RAM. At the SLS timing system one of the counters has been programmed to produce the bunch revolution clock of the storage ring and is sent on the distributed bus for transmission.

SOFTWARE

The existing EPICS device support for both EVG and EVR cards were modified to provide us with required controls over the described features [2]. The software development was made on the “eg” and “er” EPICS record/device supports, which mainly interact with the registers mapped on the VME memory via the VME bus. The new fields have been added to these records for controls and monitoring each bit or register in the hardware. They can be set/read during initialisation or at run time by database or channel access clients. The following are some of the fields which were added to “eg” record:

MDnE (Multiplexed counter Distributed bus Enable), MENE (Multiplexed counter Event trigger Enable), MCnP (Multiplexer Counter Presale), ASQ1 (AC input Sequence trigger enable), ASYN (AC input Synchronisation with multiplexed counter 7), ADIV (AC input divisor) and MSQ1 (Multiplexed counter Sequence RAM 1 trigger). Some of the fields have been added to “er” record, are as the following:

OTnB (One Time pulse distributed Bus enable), OTnB (One Time pulse distributed Bus enable) and RXVE (RX violation interrupt enable), RXVC (RX violation counter). For more explanation the reader is asked to refer to [2].

APPLICATIONS

So far we have had two different types of experiments at the SLS (e.g. FEMTO project), taking advantage of the new capabilities of the timing system. We are not going to pay attention to the details of them here.

The specific requirement of these experiments asks for a special mode of operation of the SLS machine. In the so called camshaft mode, electron beam is stored in such a way that there is a continuous chain of bunches in one side of the storage ring and a single bucket on the other side of the ring with equal time distance from head and tail of the chain of bunches.

These experiments are interested in the moment when the single bucket passes and to be synchronized with it.

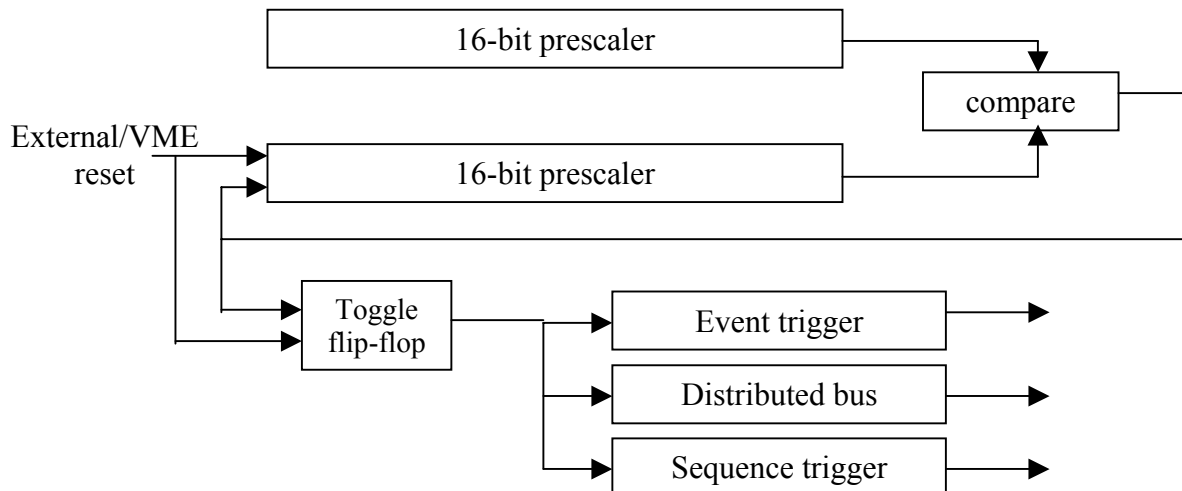


Figure 2: Multiplexed counter block diagram

What they all need to do is just installing an EVR and using the signal on distributed bus where the bunch clock is being sent by EVG. A delay unit might be needed to adjust a time delay after the received bunch clock to catch a specific bucket number. At the SLS we are using TD4V cards or DG535 Stanford delay generators for that purpose.

FUTURE PLANS

A small hardware board as an add-on to the EVR is under development and a prototype has already been tested. This piece of hardware recovers the 500 MHz clock reference (in phase with the main RF) from stream of the incoming events. That would satisfy any user (usually at beamlines) of the main RF (500 MHz)

signal around the SLS. The existing Time-Stamp driver in (EPICS) IOC core has some drawbacks. Some developments are being done to improve (by rewriting some parts of the drvTS) to overcome the problems like automatic switching between a synchronous and soft slave.

REFERENCES

- [1] <http://www.micro-researchfinland.fi/>
- [2] J. Winas, T. Korhonen, B. Kalantari, "The GlobalEvent System," Swiss Light Source, Feb. 2003.
<http://www.sls.psi.ch/controls/intranet/howto/globalEventV2.pdf>