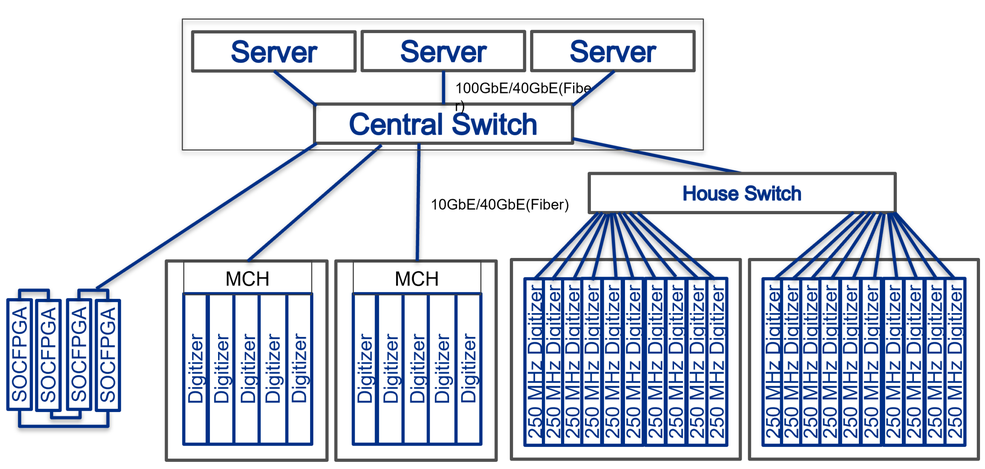
FERMILAB-POSTER-22-215-AD

A Modern Ethernet Data Acquisition Architecture for Fermilab Beam Instrumentation

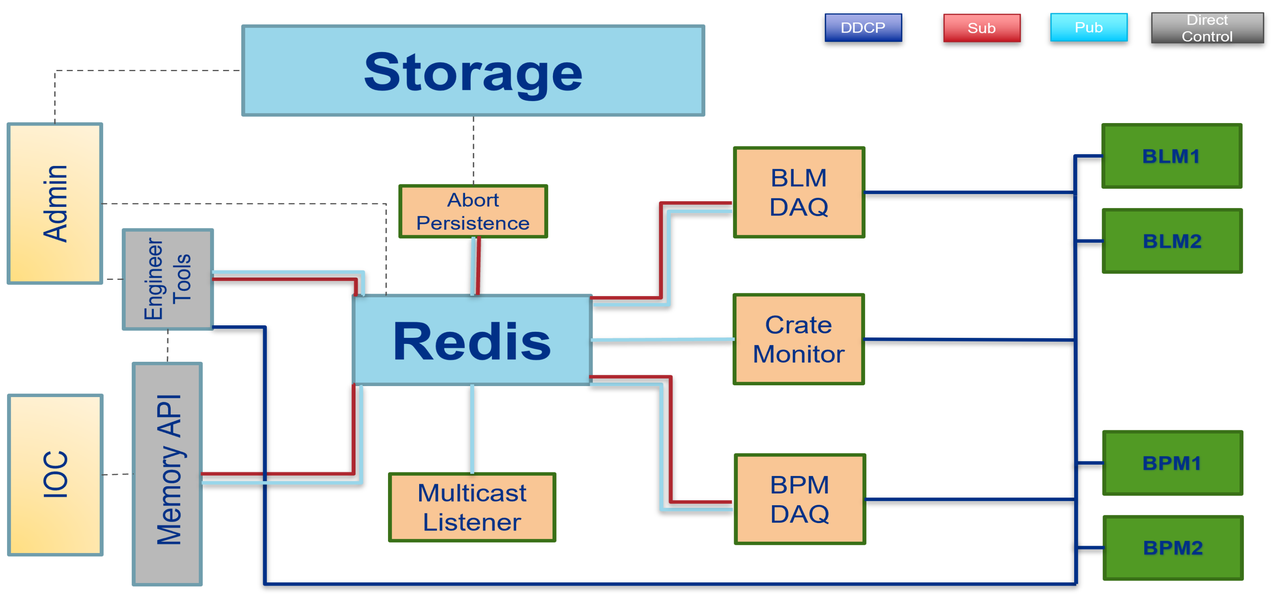
R. Santucci, J. Diamond, N. Eddy, A. Semenov, D. Voy Fermilab

Network Architecture

- Standard commodity rackmount servers and switches
- Excellent price/performance ratio
- Multiple 10Gbit Ethernet Interfaces (2-4 per server)
  - Server NIC can be upgraded and expanded
- Fiber connections to aggregated house switches
- 1GbE interfaces on edge nodes
  - 100MB/s per node with an aggregated bandwidth of ~700MB/s when nodes are read out in parallel per 10GbE interface
- Very Flexible, supporting any ethernet attached device
  - µTCA (socFPGA), Standalone PCs, VME Custom Digitizers



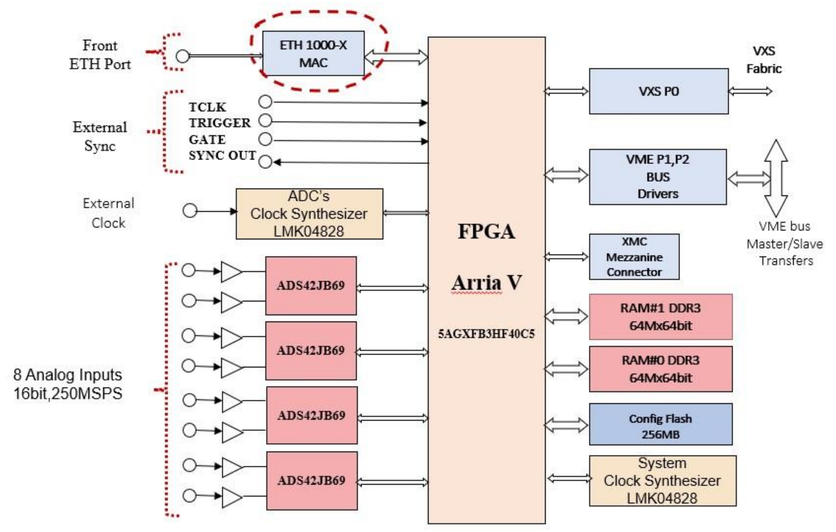
A hypothetical model showing the flexibility of ethernet as a fieldbus talking with multiple systems. MicroTCA, Standalone socFPGA , raspberry Pis, VME based custom digitizers



Software Architecture utilizing a Redis database and container-based modules

Software

- Open-Source Software
- Central Redis Database
  - Clustered to run multiple nodes across server
  - Pub/Sub for inter process communications as well as cross network communications
  - Data Streams
- Small Processing containers (Docker or Podman)
- Persistent storage on server or off server in a future Datalake
- Data hooks for controls systems (ACNET / EPICS) and user access
- Redis TCP or DDCP UDP protocols
- Embedded Linux nodes



Block Diagram for the Fermilab 8 channel 250MS/s VME/VXS digitizer. A key feature was the option to provide a Gigabit Ethernet interface from the FPGA to the front panel

Custom Digitizer

- VME form factor with Gigabit Ethernet on front-panel
- VME crate used for power and cooling
- 8 channel 250MS/s 16bit JESD204b ADCs
- Clocks locked to external machine reference
- Altera Aria V FPGA with NIOS softcore
  - Use NIOS for slow control
  - Use dedicated HDL for high-speed data
  - Use UDP to simplify interface
- Replace Device NIOS softcore with hardcore SoC
  - UDP -> TCP/IP more robust
  - Simplify device code
  - Path to increase speed 10G and beyond

Installations

- Current
  - -FAST/IOTA -PIP2IT -Muon Delivery
- Immediate Future
  - -PIP2 -Booster

The Future…

- Standard µTCA hardware platform
  - Ethernet on the backplane allows for IP addressable cards
  - IP allocation on bootup
  - Standardized socFPGA
- Very flexible Architecture
  - Devices can be anything with ethernet port
  - Single box, Crate of devices, µTCA crate, etc
  - One Controller can support many systems
  - Ethernet is not going away
    - Clear upgrade path to 10G, 40G,100G
  - Streaming applications to address future beam requirements