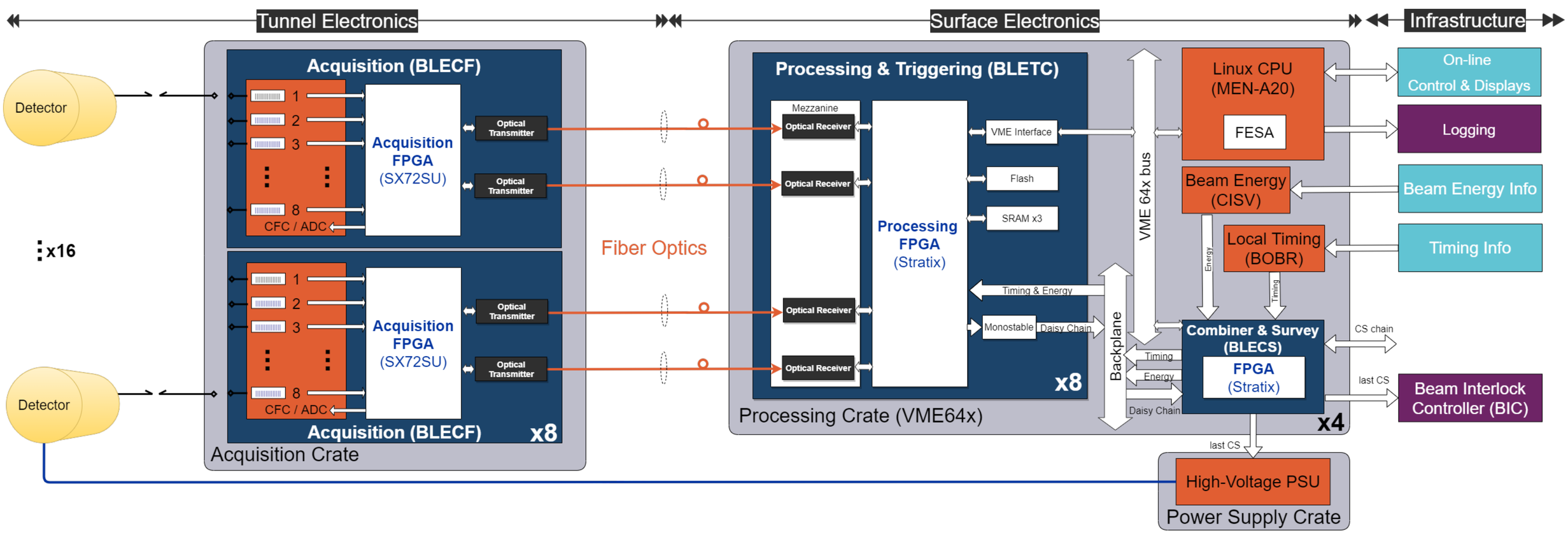
# The Beam Loss Monitoring System after LHC Long Shutdown 2 at CERN

M. Saccani*, E. Effinger, W. Viganò, C. Zamantzas, CERN, Geneva, Switzerland
mathieu.saccani@cern.ch

## Abstract

Most of the LHC systems at CERN were updated during the Long Shutdown 2, from December 2018 to July 2022, to prepare the accelerator for High-Luminosity. The Beam Loss Monitoring system is a key part of the LHC's instrumentation for machine protection and beam optimisation by producing continuous and reliable measurements of beam losses along the accelerator. The BLM system update during LS2 aims at providing better gateware portability to future evolutions, improving significantly the data rate in the back-end processing and the software efficiency, and adding remote command capability for the tunnel electronics. This paper first recall the Run 1 and Run 2 BLM system achievements, then reviews the main changes brought during LS2, before focusing on the commissioning phase of Run 3 and future expectations.

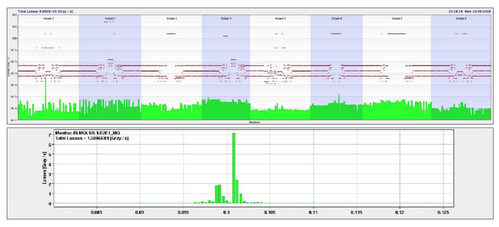
## LHC BLM System Architecture



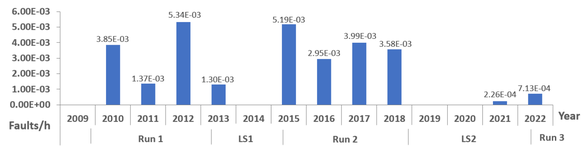

*Schematic overview of the BLM LHC system architecture.*

The LHC BLM system provides advanced diagnostics to tune beam parameters using loss patterns and locations. It is also a key part of machine protection, as a small deposition of about 100 mJ/cm$^3$ out of the 320 MJ beam energy stored in LHC can provoke a magnet quench. It can request a beam extraction in less than 3 LHC turns when excessive losses are detected. The system consists of around 4000 Ionisation Chambers, covering all the critical loss locations. They are cylindrical tubes filled with $N_2$ and hosting 1.5 kV polarized electrodes. They collect charges of secondary particles created by protons lost from the LHC beams, generating an electrical current acquired by Current to Frequency Converters. Measurements are digitised and transmitted every 40 µs to the surface. The back-end electronics located in the 8 LHC IPs provides one Gy/s value per channel on 12 different time windows, ranging from 40 µs to 83.9 s. If one of theses values exceeds a predefined threshold a beam dump is requested.

## Run 1 & Run 2 Performance



*LHC BLM fixed displays (2008).*




*BLM blocking faults per hour of LHC operation.*

The BLM system displays and stores data at 1 Hz and can save data in short buffers with 40 µs resolution on dedicated timing event triggers, such as a beam abort request. The LHC protection requires SIL3, from the beginning a huge effort was put in achieving high dependability, but decreasing the availablity in the first runs.

## LS2 Changes

Table 1: BLM latencies† measured at Run 3 commissioning.

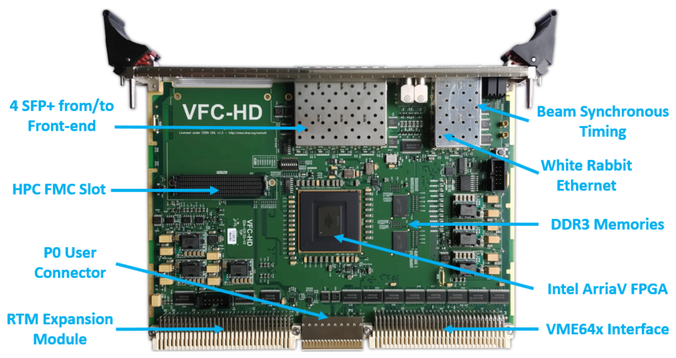
| LHC Interaction Point | Beam 1 | Beam 2 |
|---|---|---|
| IP1 (ATLAS) | 46 µs | 44 µs |
| IP2 (ALICE + B1 inj.) | 41 µs | 41 µs |
| IP3 (Momentum Cleaning) | 61 µs | ~114 µs†† |
| IP4 (RF) ††† | - | - |
| IP5 (CMS) | 30 µs | 53 µs |
| IP6 (B1 & B2 Dump) | 35 µs | 32 µs |
| IP7 (Betatron Cleaning) | 64 µs | 88 µs |
| IP8 (LHCb + B2 inj.) | 56 µs | ~177 µs†† |

† Injection kick top to dump request, time of flight corrected.
†† Stretched because of RC filter installed on the detector.
††† No collimator at IP4.

During LS2, 30% of the detectors were re-installed, 15 acquisition cards exchanged, WorldFIP receivers deployed, 44 processing cards replaced. A new optical receiver mezzanine was designed. A firmware overhaul extensively verified in simulation led to a portable and high-performance implementation. The CPU OS was migrated to CentOs7, and consequently FESA, and drivers. The whole BLM application suite. The BLM latency was measured again after the upgrade and meets the specification.

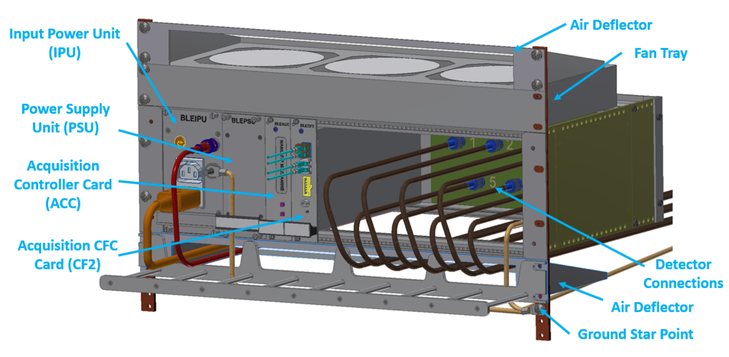
## LS3 & LS4 Expectations

This new board, called VFC-HD, is a BI standard back-end module to be installed in a radiation-free area. It will be used as a VME-based unit for data concentration and processing, providing 4 standard SFP+ transceivers and additional processing resources to improve efficiency and flexibility, and strengthen critical parts by using redundancy for example. In addition, extensive testing, burn-in and run-in were carried out after manufacture on a sophisticated test bench to verify the 1150 assets produced before being installed.



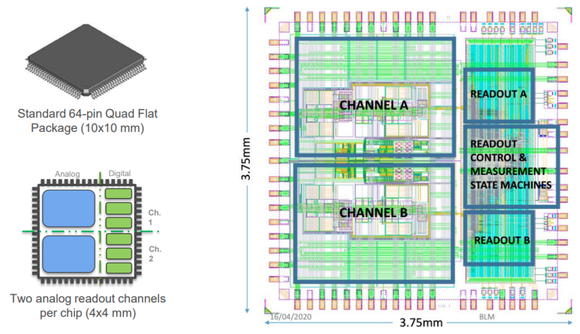

*Overview of the VFC-HD features.*

A new acquisition electronics under development will be deployed in SPS in LS3, and reused in LHC in LS4. It will reduce the time resolution to 5µs (was 40µs), increase radiation tolerance to 1KGy (was 500Gy), and ensure user safety and SIL3. This 3U acquisition crate is composed of a special backplane that hosts 8 signal inputs from the detectors, an input power unit with a 230 $V_{AC}$ transformer, a power supply module generating local voltages, a crate controller with a nanoFIP fieldbus connection, and the modernised CFC board.




*3D view of the future acquisition crate.*

A new front-end ASIC will allow to withstand radiation doses up to 500 kGy (was 500 Gy), to place electronics closer to the beam and minimise the noise from cables. The chip consists of two independent channels readout by redundant blocks interfaced to LPGBT. Using a CFC combined with a Wilkinson ADC, the ASIC provides a 10 µs readout (was 40 µs), and can request a beam dump in less than 1 turn. Characterisation tests on prototypes, including irradiation campaigns, showed that the device can perform loss measurements down to 1 pA with an error below 1% in the range [35 µA;1 mA].




*Overview of the BLMASIC chip architecture.*

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