ISBN: 978-3-95450-241-7 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2022-WEP14

CAVITY BPM ELECTRONICS FOR SINBAD AT DESY

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Abstract

The SINBAD (Short and INnovative Bunches and Accelerators at DESY) R&D accelerator is planned for studying new concepts for high gradient electron beam acceleration and the generation of ultra-short electron bunches. The accelerator called ARES (Accelerator Research Experiment At DESY) is composed of S-band accelerating structures. In order to achieve the goal of very short electron bunches the electron beam charges generated in the RF (radio frequency) Gun can vary in a range from 200 pC down to 500 fC. A new type of high resolution cavity BPM (beam position monitor) has been developed to measure the beam position with good resolution at small charge down to 500 fC. One key component in the BPM system are the custom RF front-end receiver electronics to meet the resolution requirements in the required charge range. The entire BPM system with a focus on the system design requirements and the MicroTCA based RF electronics are presented in this paper.

INTRODUCTION

The S-band electron linear accelerator ARES at DESY in Hamburg, Germany is build for studying novel acceleration techniques including a beam manipulation testbed, accelerator components and concepts for autonomous accelerator operation. Its target parameters are an energy of 50 MeV-155 MeV, a charge of 0.5 pC-200 pC. A single electron bunch at the rate of 50 Hz is generated by an RF-Gun in which the electrons are released from a cathode by making use of a photocathode laser. The machine has already been successfully commissioned and first experiments have been carried out [1–4]. The diagnostics include eight high resolution in-house developed cavity BPM (beam position monitors) which are distributed at significant locations along the 50 m long machine [5] . An overview of the machine with two BPMs currently under test is shown in Fig. 1.

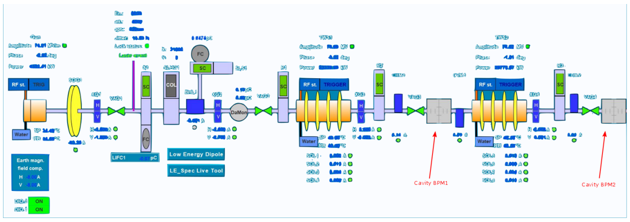

Figure 1: Extraction from ARES Linac operation panel with two cavity Beam Position Monitors.

The key specification of the cavity BPM system are position measurements at bunch charges from 500 fC up to 1 nC. The challenging requirement in precision and accuracy at the smallest charge is 5 µm in a measurement range of 100 µm while averaging over 25 bunches. The single bunch resolution requirement over a range of 700 µm is 35 µm [6].

CAVITY BEAM POSITION MONITOR

In order to determine the bunch charge and position of the electron bunch in the beam-pipe a monopole and two dipole excited modes in the cavity are necessary [7, 8]. The excited monopole mode shows a proportionality to the electron bunch charge and two excited dipole modes deliver proportionalities to the horizontal and vertical position of the electron bunch. The measured voltages are $V_{mon} \propto q$ and $V_{dipole} \propto x_{pos}, y_{pos}$ respectively. The realization of the cavities for measuring the amplitudes of monopole and dipole modes are based on a tedious design procedure of the vacuum chamber which includes electromagnetic field simulation and tolerance studies before it could be produced. More details can be found in [9]. A simplified electromagnetic simulation model of the cavity is shown in Fig. 2.

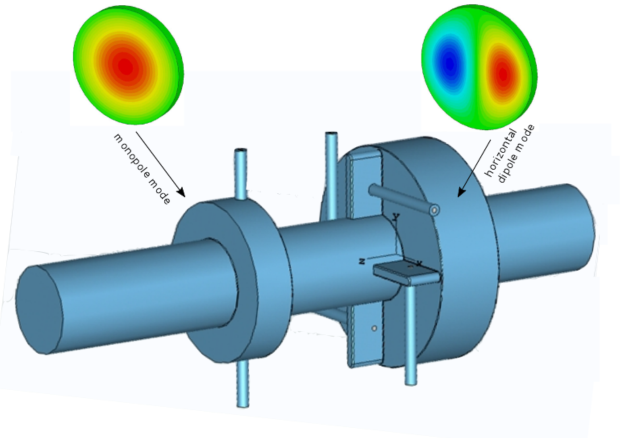

Figure 2: Simulation model of Cavity Beam Position Monitor. Monopole and dipole modes have symmetric ports to maintain symmetric fields around the beam axis. The measurement system only uses one of the ports and the other is terminated with 50 Ohm.

The mono and dipole cavity geometries have been chosen to be compatible with existing BPM monitors already installed at the E-XFEL and FLASH at DESY, Hamburg, Germany. Both machines operate with high repetition rates of the electron bunch of up to 4.5 MHz. Therefor a loaded quality factor of around 70 has been a feasible choice to avoid an overlap of subsequent bunches. The design procedure also aimed for high sensitivities of monopole and dipole cavities to deliver sufficient signal power at very low charges.

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Significant characteristics of the cavity BPM resonators are summarized in Table 1.

Table 1: Design characteristics of monopole and dipole cavity.

Quality	Quantity
Resonance frequency f_0	3.3 GHz
Loaded Quality Factor Q_L	70
dipole Sensitivity S_{dip}	4.25 Vpk/nC/mm
monopole Sensitivity S_{mon}	43 Vpk/nC

ACQUISITION SYSTEM

The acquisition system is composed of a custom-made heterodyne RF front-end receiver, a COTS (custom of the shelf) digitizer board [10] including analog-digital converters (ADCs) and an FPGA (Field Programmable Gate Array) for pre-processing the data. A machine synchronous interrupt driven server application receives the data from the FPGA via backplane in the MicroTCA [11] crate. The signal flow of the analog signals is shown in Fig. 3.

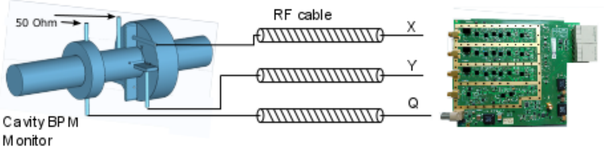


Figure 3: Analog signal flow.

A MicroTCA platform including digitizers, FPGA, CPU and timing system for the eight cavity BPMs installed in ARES is shown in Fig. 4.

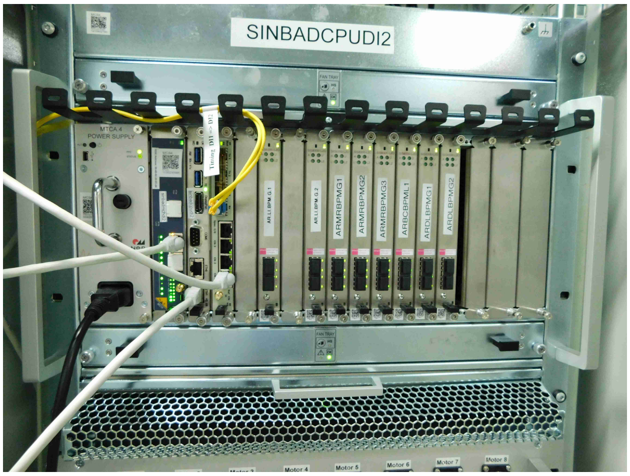


Figure 4: MicroTCA crate with digitizers, CPU, MCH, and timing system.

RF Front-End Receiver

The RF front-end receiver is composed of three equal channels and a LO (local oscillator) block. The RF signals from the cavity are band-pass filtered and can be amplified by a factor of 52 dB at the center frequency of 3.3 GHz. Step attenuators with a range from 0 - 31.75 dB make it possible to adjust the gain for different charges and make sure that the following down-conversion stages are not over-driven. During machine commissioning for different experiments the switching process of attenuators is negligible for the accuracy of the position calculation. After the amplification stages the cavity signals are demodulated to a base-band signal with the help of a synchronous LO signal at 3.301 GHz. This LO signal is generated with a software configurable integer-N phase locked loop. The base-band signal contains two independent paths for I and Q components which are delivered by the demodulator. These signals are buffered with a differential driver amplifier and are then send to the digitizer board. The minimum expected signal power for the dipole cavity resonator at a charge of 500 fC is -89 dBm with an offset position of 10 µm from center. The minimum signal power of the monopole mode cavity is -30 dBm. These expected powers levels include the RF cable losses. An RF channel isolation of better than 100 dB has been achieved. This is necessary in case of large monopole signals and very small dipole signals. A simplified block diagram of the RF front-end is shown in Fig. 5.

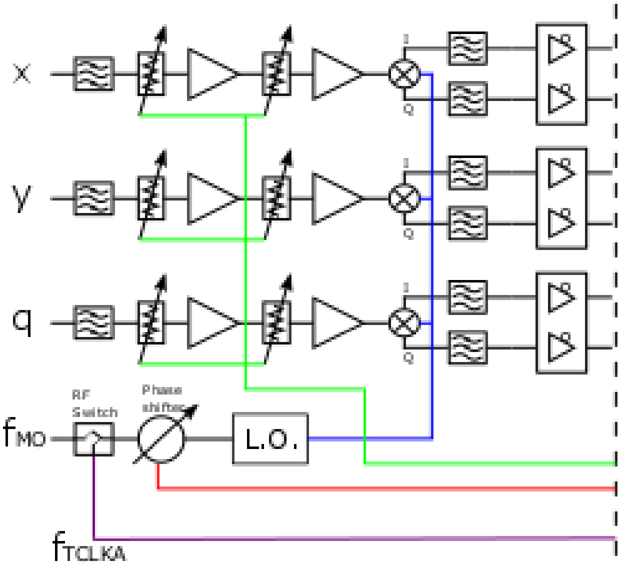
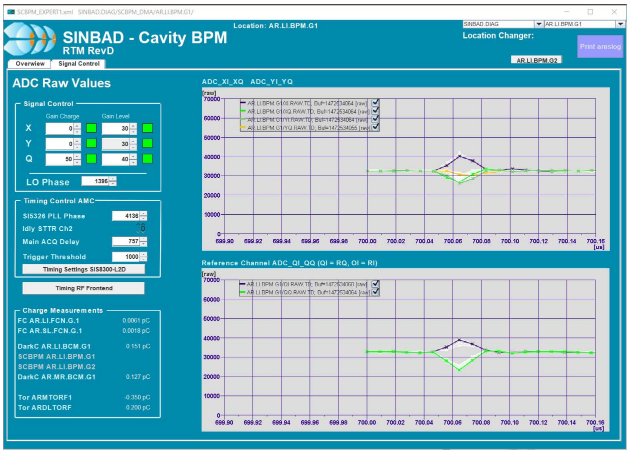


Figure 5: Block diagram of the RF front-end receiver. Green: SPI bus to adjust step-attenuator settings. Blue: LO distribution. Red: LO phase adjustement.

Firmware and Server Application

The signals from the RF front-end are digitized at a rate of 125 MHz and 16 Bits. A custom firmware to arrange the raw ADC data for further processing is implemented in an FPGA. It also includes several interfaces to the programmable RF front-end components such as an SPI interfaces for the step attenuators and PLL, an I2C interface for a DAC to adjust the LO phase with a phase shifter and several switchable gains in the x,y, and q measurement channels. Currently the adjustment of the waveforms with respect to the ADC clock is done manually. A raw data waveform and interface server are displayed in Fig. 6.


SCBPM_EXPERT1.xml SINBAD.DIAG/SCBPM_DMA/AR.LI.BPM.G1/

Location: AR.LI.BPM.G1

Location Changer: SINBAD.DIAG / AR.LI.BPM.G1

Signal Control

	Gain Charge	Gain Level
X	0	30
Y	0	30
Q	50	40

LO Phase 1396

Timing Control AMC

SI5326 PLL Phase	4136
Idly STTR Ch2	0
Main ACQ Delay	757
Trigger Threshold	1000

Charge Measurements

FC AR.LI.FCN.G.1	0.0061 pC
FC AR.SL.FCN.G.1	0.0018 pC
DarkC AR.LI.BCM.G1	0.151 pC
SCBPM AR.LI.BPM.G1	
SCBPM AR.LI.BPM.G2	
DarkC AR.MR.BCM.G1	0.127 pC
Tor ARMTORF1	-0.350 pC
Tor ARDLTORF	0.200 pC

AR.LI.BPM.G1/XI.RAW.TD; Buf=1472534064 [raw] ☑
AR.LI.BPM.G1/XQ.RAW.TD; Buf=1472534064 [raw] ☑
AR.LI.BPM.G1/YI.RAW.TD; Buf=1472534064 [raw] ☑
AR.LI.BPM.G1/YQ.RAW.TD; Buf=1472534055 [raw] ☑

AR.LI.BPM.G1/QI.RAW.TD; Buf=1472534060 [raw] ☑
AR.LI.BPM.G1/QQ.RAW.TD; Buf=1472534064 [raw] ☑

Figure 6: Signal control interface with step attenuator and gain settings, ADC timing, acquisition delay adjustment.

The calculations applied on this waveforms are implemented in a text-file based python script. The charge calibration has been cross-referenced with charge readings while the horizontal and vertical calibration have been made with magnetic steerers and a screen. Both are hard-coded in the python script. One pre-requisite of the proper usage of the system is a phase control loop which keeps the phase of the monopole q channel at an angle of 45°. Another pre-requisite is the alignment of the x and y vectors with respect to the reference channel. With this correction beam position and beam angle can be separated and the orientation of the coordinate system is adjusted.

MEASUREMENTS

First measurements with electron beam at ARES have been made and indicate promising results. The first two BPMs have been calibrated with the help of a screen and a steerer. The linear measurement range exceeds > +/- 5 mm. The standard deviation of position fluctuations including beam jitter is better than 10 µm at a charge of 1.25 pC.

CONCLUSION

Compact cavity BPM electronics can be realized with the MicroTCA form factor. Measurements at charges smaller than 1 pC is possible. The standard deviation of position measurements at these small charges fulfill the specifications. A proper implementation of the algorithm in a server platform for the control system is under way and will improve the stability and usability of the measurement system.

ACKNOWLEDGEMENTS

The authors are very grateful for tremendous support and exchange of conceptual and technical ideas with collaborative colleagues from Paul Scherer Institut (PSI) in Switzerland. Particularly these are G. Marinkovic and M. Stadler.

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[11] MicroTCA.4 specfcations source, `http://www.picmg.org`