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# Methodology, Characterisation and Results from the Prototype Beam Loss Monitoring ASIC at CERN

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## Abstract

The characterisation of novel beam loss monitoring front-end converters, based on radiation-hardened application-specific integrated circuits (ASIC), is undergoing at CERN. An effective performance analysis of the newly developed ASICs plays a key role in their candidacy for the future installation in the HL-LHC complex. This work introduces the latest test-bed architecture, used to characterise such a device, together with the variety of audits involved. Special focus is given on the verification methodology of data acquisition and measurements, in order to allow a detailed study of the conversion capabilities, the evaluation of the device resolution and the linearity response. Finally, the first results of post-irradiation measurements are also reported.

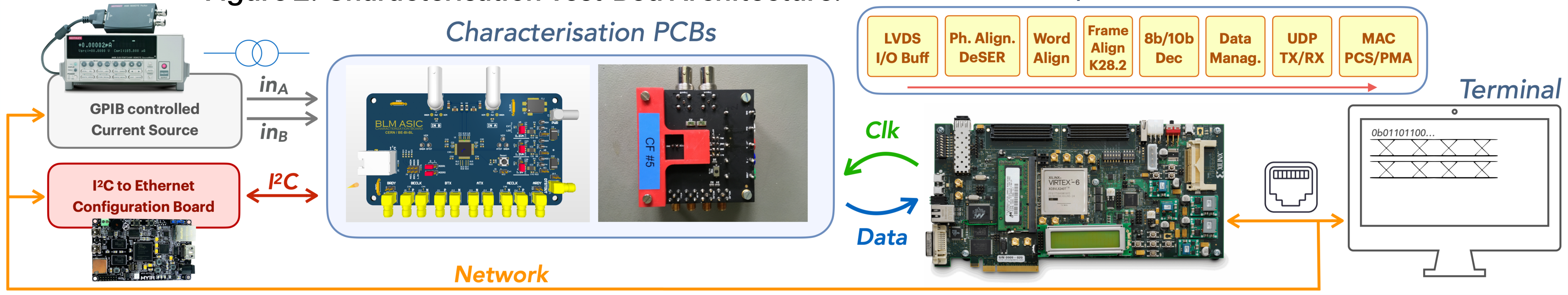
## Introduction

The Beam Loss Monitoring (BLM) is an essential protection system of particle accelerators, since it prevents equipment damage, and the quench of the superconductive magnets (as in LHC), in case of unwanted loss particle energy depositions outside the beam pipes. In view of the HL-LHC upgrade, major renewals of the BLM electronics are planned, requiring enhanced radiation tolerance front-ends (up to 100MRad TID), faster response to high losses (down to 10μs) and better noise performances (< 1pA). This has demanded the development of a new BLM Application Specific Integrated Circuit (BLMASIC), able to convert the detector analogue currents into digital data streams, which are transmitted to the back-ends by optical fibres. Strict validation tests and performance characterisations are required for such a device, carried-on at the SY-BI-BL laboratories. The device conversion architecture, the involved methodology and first post-irradiation results are reported.

## Conversion Architecture

The BLMASIC-CFCv2 has been used in this test-bed. Its conversion architecture (Fig. 1) is based on a current-to-frequency converter. It synthesises a triangular waveform and, by using a counter, measures its frequency, which is proportional to the input current intensity. A next processing allows to yield the resulting losses. Furthermore, an auxiliary Wilkinson ADC directly monitors the waveform value, to improve the measurement speed and the resolution.

Figure 2: Characterisation Test-Bed Architecture.



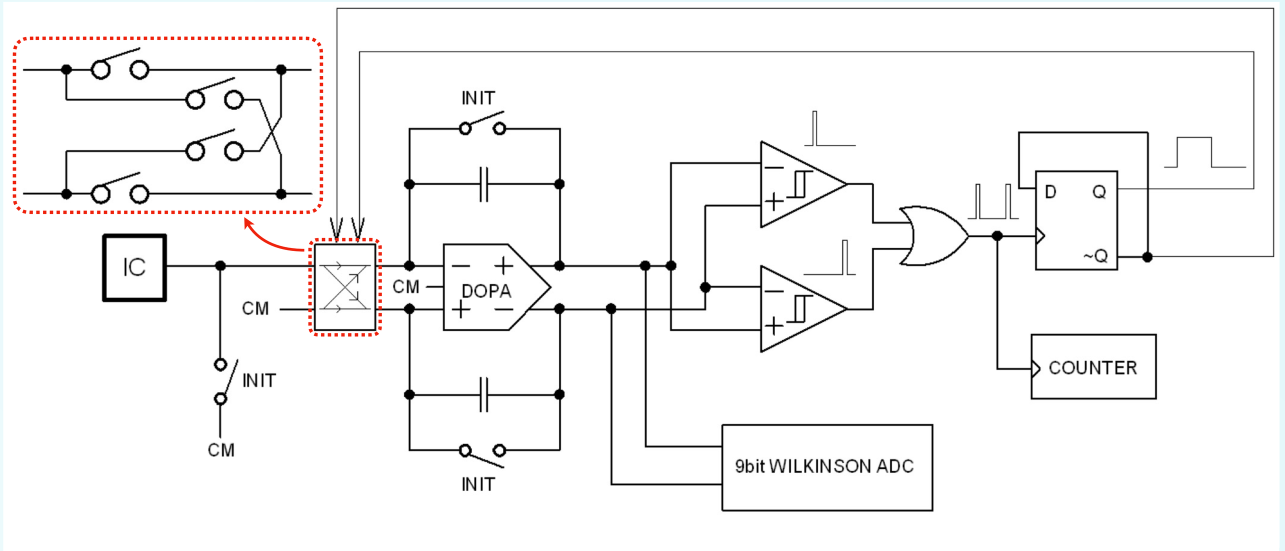




Figure 1: BLMASIC-CFCv2 Conversion Architecture.

## Methodology

### Basics Device Functionality Tests

Initially, the rail currents and the power consumptions are measured ($P_{tot}$ = 71 mW). Then, simple queries are performed on the I²C configuration interface and validated by using a logical protocol checker. Thus, the fast output data lanes are connected to an oscilloscope and the 8b/10b decoder, included in this latter, has allowed to validate the data frame compliance and to retrieve the first raw results. Finally, reset events and power cycles are tested, verifying the reliability of the device boot. An internal dead-lock state issue has been observed at slow power-up ramps. This has been corrected in the newest BLMASIC-CFCv3.

### Conversion Performances

The test-bed (Fig. 2) has been assembled to inject calibrated current sweeps into the device and to monitor simultaneously its internal registers content. The output lane is now connected to a properly programmed FPGA board, providing the clock and the data acquisition. For each testing current, the overall device memory content is stored on a terminal PC. Data are transmitted to it by using UDP based packets over a gigabit Ethernet interface. We stored:

- 50 acquisitions from 1pA to 1nA, of 10s each,
- 500 acquisitions from 1nA to 1mA, of 1s each.

### Device Irradiation

Total ionisation dose (TID) and single latch-up / event-upset (SEL / SEU) tests need to verify the correct behaviour of the irradiated circuits and the specifications compliance. In a preliminary study we compared one brand new device with five others irradiated with X-Rays (performed at EP-ESE-ME). Afterward, other sources will be used, such as: high-energy protons (at the PSI) and mixed field radiation (at CHARM - CERN).

## Data Analysis & Results

The raw data require a pre-processing, to collect the measure registers and produce convenient forms. Since computationally expensive, because of bit-addressing, a specific parallelised software has been developed. Later, to compute the device conversion characteristic and its error, a procedure is designed. Due to the input high dynamic range (180dB) and to stay within the desired precision, several measurement durations are considered: < 100μs for currents > 10μA, > 10s for currents ~1pA. The procedure consists in: 1. partitioning of the full samples in clusters of the specified time window; 2. averaging of the data within each of the cluster; 3. the computation of the standard deviation amongst all averaged measures; 4. computation of all samples average, representing the reference result. The Wilkinson ADC data follows a similar procedure, in which step 2 is replaced by computing the waveform trough a linear regression. Clusters including direction swaps are discarded. Fig. 3 shows a relevant result obtained for high currents with CFC counter data only. It reports the measured versus the injected current.

No major performance drifts have been observed amongst the devices. The ripples in the error plot seem due to the data processing, not reflecting physical phenomena. Relative errors have been computed by combining the data of the two plots. It turns out that a measurement error smaller than the 10% is observed for currents greater than 3μA, while it stays below the 1% for currents above 35μA. This is well inside the design specifications and it can be improved by advanced filtering techniques. Finally, a deviation from the linearity has been observed, which degrades the accuracy for currents in full-scale regime. This is due to a connection bug in the input stage clamping diodes, which has been solved in the v3 upgrade.

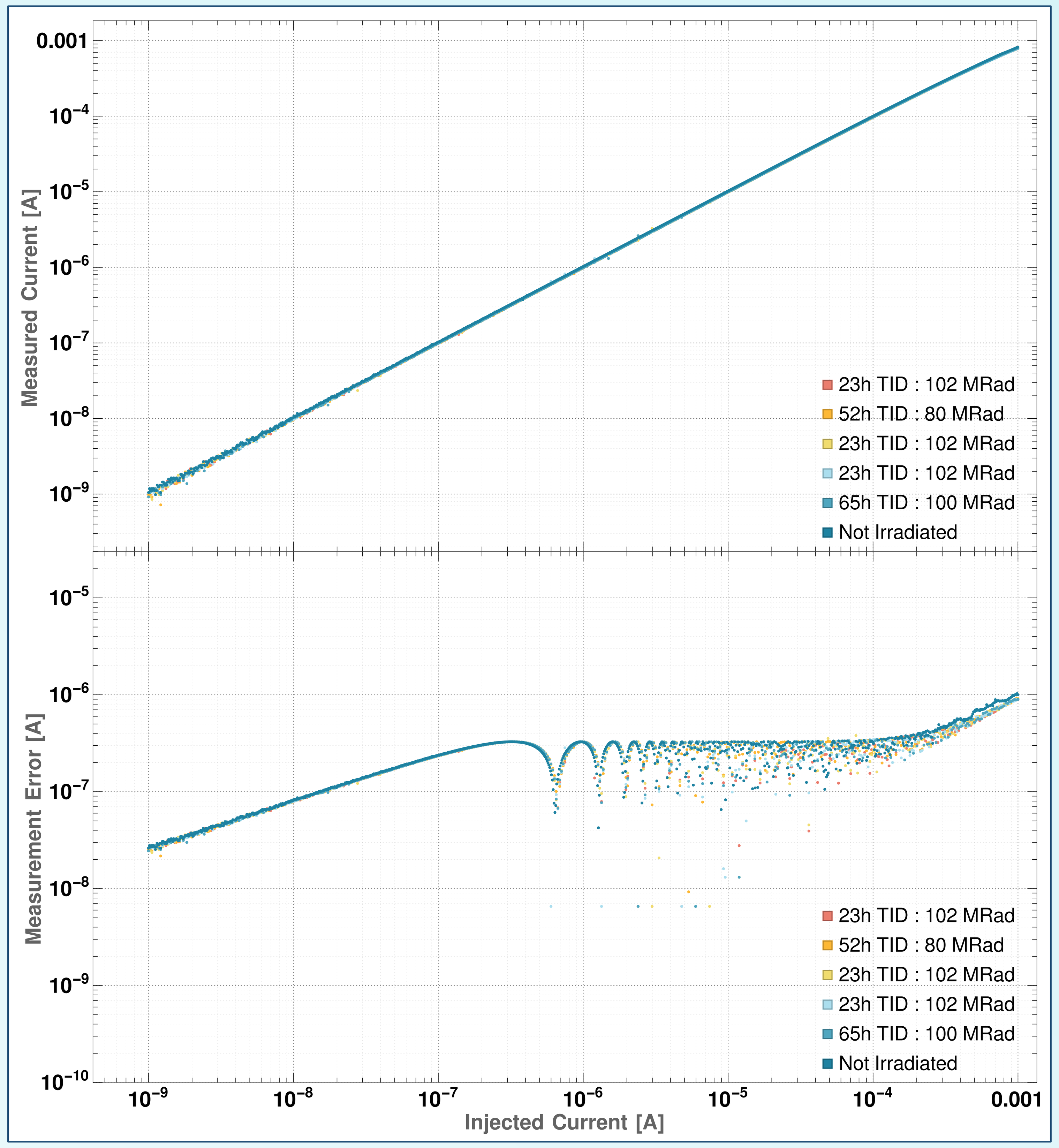



*Figure 3: Conversion characteristic (top) and absolute errors (bottom) by a logarithmic current sweep of 500 values from 1nA to 1mA. The averaging time window is set to 100μs.*

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