Testbed Development for the Characterisation of an ASIC for Beam Loss Measurement Systems

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Abstract

A high-performance, radiation-hardened, application-specific integrated circuit (ASIC) is under development at CERN for digitising signals from beam losses monitoring systems in harsh radiation environments. To fully characterise and validate both the analogue and digital parts of these ASICs, an automated testbed has been developed. Here we report on the components used to build this set-up, its capabilities as well as the methodology of the data analysis. Focus is given to the data collection, the automation and the efficient computation methods developed to extract the merit factors of two different ASIC designs from prototype manufacturing runs.

Introduction

In view of the HL-LHC upgrade [1], our team is developing a new version of Beam Loss Measurement (BLM) electronics. This is a critical system which protects the particle accelerators against damage or quenches [2], caused by lost beam particles producing an excessive secondary cascade radiation [3].

The new key component of this BLM front-end, as compared to the old system [4-6], is a custom-designed Application Specific Integrated Circuit (BLMASIC), which will guarantee high resolution measurements in harsh radiation areas, where off-the-shelf components cannot be used.

The general aim of the present research is to validate the specification requirements for the ASIC (e.g. the linearity behaviour, the resolution, the temperature stability, the radiation/fault tolerances etc.) and to compare two different device architectures: one is based on the same concept of the operating system (current-to-frequency converter, BLMASIC-CFC), the other one would implement a delta-sigma converter (BLMASIC-ΔΣ). The results of the comparison will lead us to choose the most suitable device for the final installation.

This work focuses on the architecture and assembly of a smart testbed to perform this tests, including: the design of a characterisation board, the selection of suitable laboratory instrumentation, the development of the acquisition firmware, as well as the software for batch data analysis.

Testbed Architecture

In order to validate the performance of the BLMASICs, we have designed a characterisation PCB, which allows us quick access to the device interfaces and debug features (Fig. 1). The board is equipped with low leakage BNC inputs, used to inject the test currents into the device; redundant SLVS lanes to provide the clock and output the data stream; an I²C bus to read and configure all the internal registers; three diagnostic

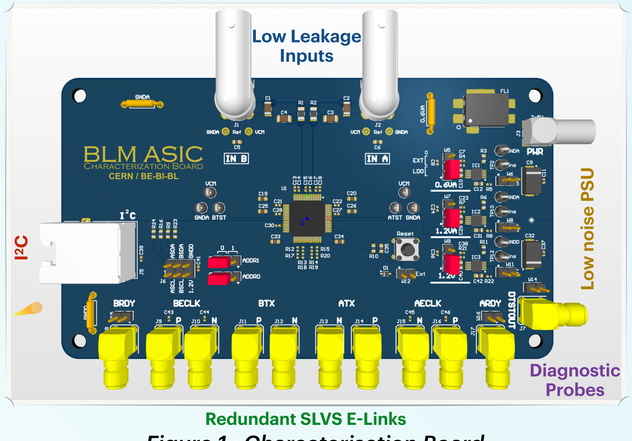

Figure 1 : Characterisation Board.

probes connected to a programmable multiplexer, switching among several internal analogue and digital signals. The card can be powered by external supplies or by the low noise embedded ones.

The high accuracy and robustness requirements for the final product were taken into account during the selection of the components and the PCB manufacturing technology. Furthermore, in order to perform irradiation tests, a version with the suitable electronics has also been designed.

The architecture of the complete testbed used for the measurements is shown in Fig. 2. The standard CERN Beam Instrumentation VME FMC Carrier Board (VFC-HD) FPGA [7] runs the firmware to acquire the real-time data. In the testbed, it performs the 8b/10b data stream decoding and reads the measurement values. Then, an external logic analyser is connected to the carrier board, which dumps, driven by a MATLAB script, the acquired data on a computer file. The same script is able to program the internal registers of the BLMASICs and to configure the test-current source. The required clock is provided by an external FPGA board. To verify particular BLMASICs working conditions needing real-time data tracking, additional firmware modules have been developed.

Each of the testbed instruments is directly connected to the CERN internal network, or through a computer set up for the tests. This architecture makes it possible to run automated measurement sessions and to control the overall system remotely, even when the operators are teleworking (e.g. due to COVID-19).

Data Analysis

We have exploited the testbed to verify the basic device operation: the power consumption, the initialisation procedure and the digital interface functionalities. Furthermore, we tested the analogue-to-digital conversion performances, such as the electronic noise estimation and resolution characterisation. These often require hundreds of seconds both in the data acquisition and in the processing, because many samples are needed for high resolution. Thus, a C++ multi-threaded batch data analysis has been implemented, optimising the operations on multi-core computers. This has allowed us to reduce the computational time from many hours to less than ten minutes. The analysis includes: 1. Loading the sample file, 2. Sample clustering in groups of specified size (a certain time window), 3. Averaging within each group, 4. Standard deviation computation among all the averages, 5. Iteration of the procedure for different group size.

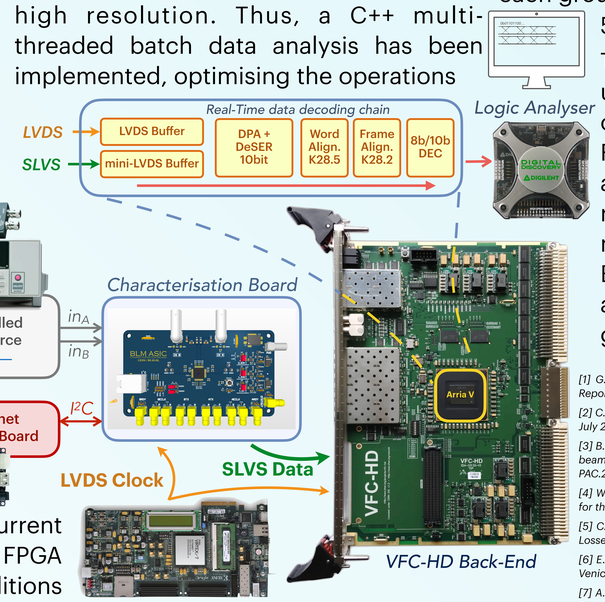

Figure 2 : Testbed Assembly.

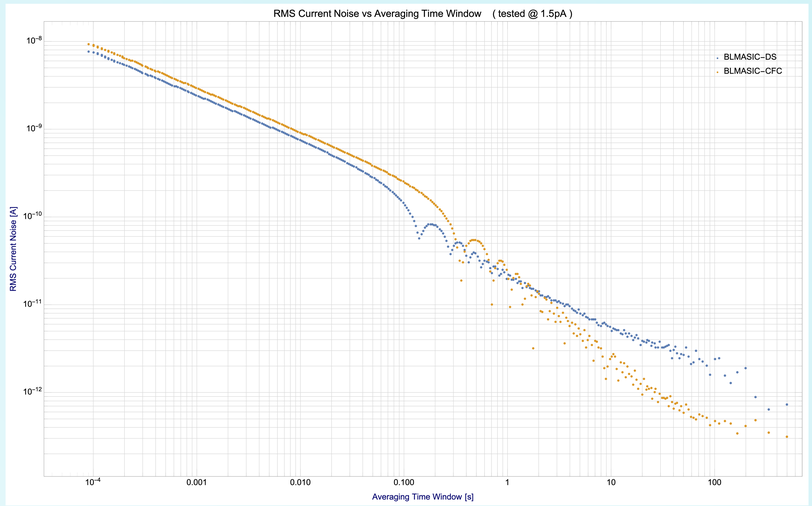

Figure 3 : Example of current measurements noise characterisation vs. averaging time window. BLMASIC-DS in Blue, BLMASIC-CFC in Orange.

The relevant information about electronic noise limits helped us to evaluate the needed averaging time in correspondence of a given precision. A result of this method is reported in Fig.3. Fluctuations appearing for ATW > 10s can be smoothed acquiring data for a longer time. As we expected, the plot reaches a plateau for longer periods, since the measurement noise goes to the electronic limit. However, since the BLMASICs specifications require an electronic $rms_{noise} \leq 1$ pA, already from these preliminary results, one can see that the goal has been achieved for time windows > 200s.

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