A Common Diagnostic Platform For Elettra 2.0 and Fermi

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In a previous paper we introduced a prototype of an electron Beam Position Monitoring system based on pilot-tone compensation, fully integrated in the Global Orbit Feedback system (GOF) of Elettra. In order to separate the analog and digital subsystems of the prototype, a modular design has been implemented. In this manner we had the chance to design, test and improve the analog signal conditioning subsystem, whose main goal was to feed any suitable digital acquisition system.

For the first in-house evaluation of the front end, we put together a set of evaluation boards that globally acted as a digitiser; the drawback of this approach was the phasing out of various constituting devices. The evident lack of technology which was lived up to expectations, pushed us to develop in-house a suitable board with conversion and processing equipment powerful enough to be adopted as a generic board for a number of different applications.

Taking into account that the operation of both accelerators (Elettra and Fermi) relies on old equipment whose failure rate is supposed to increase over time, the design of this new generic board fulfils two goals: upgrade the full set of Elettra BPMs in the short time, replace the remaining acquisition systems in the long time.

Replacing diagnostics in Elettra and Fermi

Since their first operation (1993 Elettra, 2010 Fermi), both lightsources rely on various equipment fully developed and built in-house. Due to ageing, it is mandatory to service partially or totally the installed equipment; this is the list of the systems involved in diagnostics tasks that need to be refitted:

- Low-Level RF system (Elettra);
- RF Cavities Monitor (Elettra);
- Beam Dump Monitor (Elettra);
- Cavity Beam Position Monitor (Fermi);
- Bunch Arrival Monitor (Fermi);
- Link Stabilizer (Fermi).

Even if the purposes of these systems are very different among them, they share several aspects from the electronics point of view: acquiring input signals (analog and/or digital), performing processing, transmitting data to the control system and, when required, generating local outputs (analog and/or digital). If the analog treatment of the signals and the AD/DA conversion tasks are detachable, a digital platform designed in a modular way can be shared among many different applications.
Furthermore, the modular approach is well-suited to Elettra and Fermi control systems topology that acquire data by distributed sensors and perform in a centralised server all the calculations required to drive the actuators in order to maintain stable the beams orbit. The Cavity BPMs, for example, send the acquired waveforms to the control system CPU over a standard Gigabit Ethernet link and not via the microTCA backplane, allowing physical separation between acquisition and calculation equipment even over long distances.

Digital platform for eBPM

In a previous paper, we introduced a prototype of an electron Beam Position Monitoring system based on pilot-tone compensation, fully integrated in the Global Orbit Feedback system (GOF) of Elettra. The prototype is based on an Altera Stratix III FPGA, whose functional blocks are:

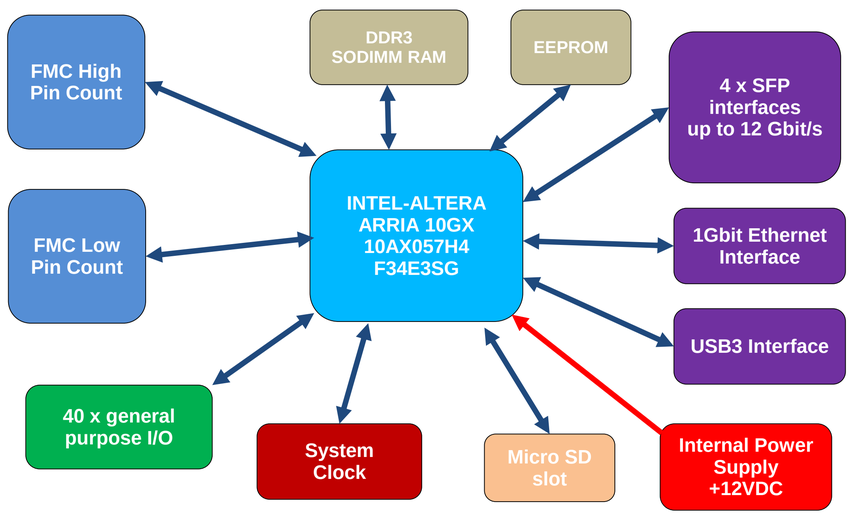
- two separate digital receivers (one for beam signal, one for the pilot tone) with CIC and FIR filters;
- two UDP Ethernet cores with SFP modules (Gigabit Ethernet);
- an external memory controller (1 GB of DDR2).

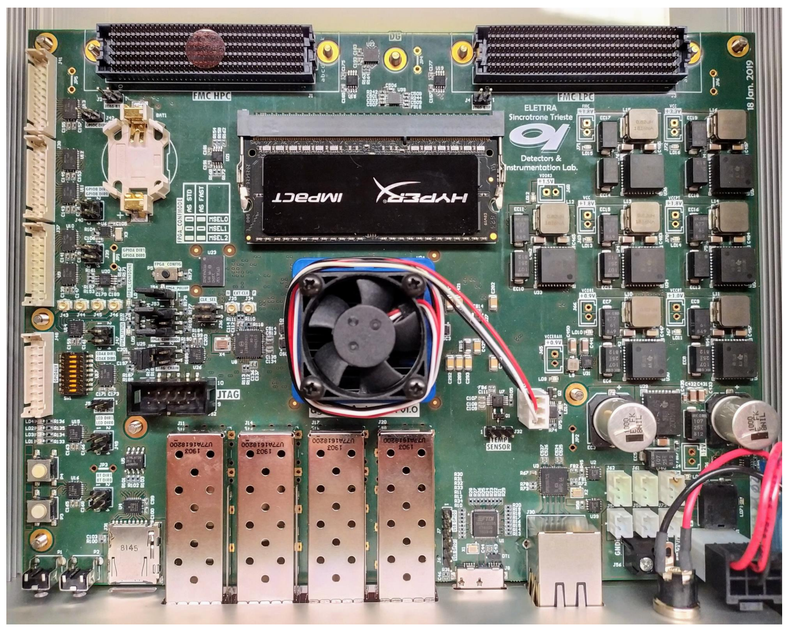
That design uses about 50.000 logic elements, 2 Mbit of embedded memory (FIFOs) and 88 DSP blocks. The incoming signals are digitised by four LTC2209 (16-bit, 160 MS/s), driven by a low jitter sampling clock synchronised with the machine clock of Elettra. The new eBPMs, based on the incoming platform, should:

- house two complete BPM systems, optimising hardware, logic resources and interlock capabilities (angle detection);
- collect ADC raw data in a DDR SDRAM for post mortem and turn-by-turn beam analysis;
- share the acquired data by high speed links for reduced latency (10 Gbit/s);
- undersample the inputs by high-linearity 16-bit ADCs;
- drive the ADCs with a low jitter clock synchronised with the external reference (machine clock);
- export several digital I/Os (trigger, interlock, post mortem, …);
- use four LTC2107 ADCs (16-bit, 210 MS/s). They have been already tested on an in-house developed FMC module and have shown better overall performances than the previously adopted LTC2209.

New platform

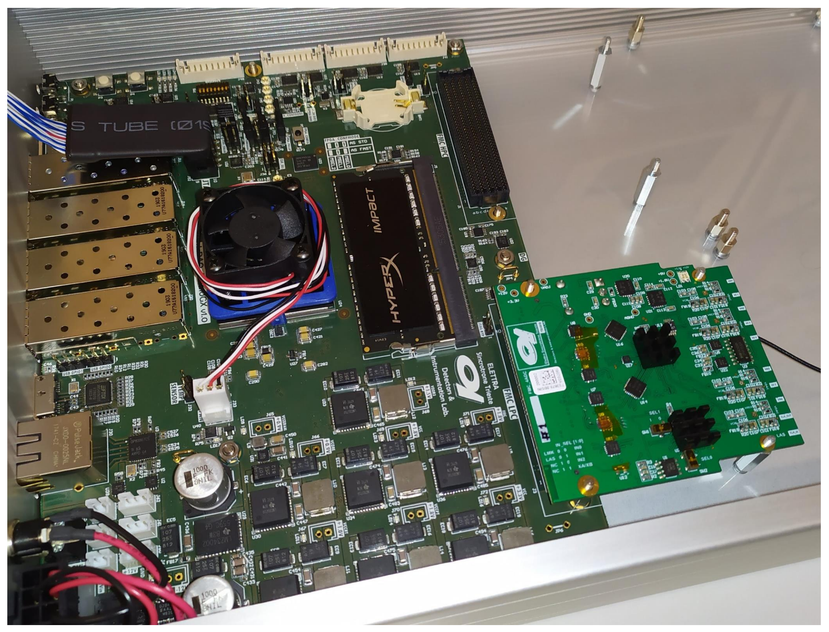
Following the modular concept, we are developing a brand new platform called dgDAQ, whose core is an Altera/Intel Arria 10 570 GX FPGA, with 570.000 LEs (logic elements), 868.000} registers, 3046 DSP blocks, 35 Mbit of embedded memory, 24 transceivers capable of 12.5 Gbit/s, 1152 pins with 222 LVDS pairs.
The FMC connectors are the key feature that gives the demanded flexibility: in fact the specific final configuration of the system essentially depends on the installed FMC module. For example, in the dual eBPM case, two FMC modules with 4 ADCs are necessary, whereas for dual Cavity BPMs, two FMC modules with 2 ADCs and 2 DACs are to be mounted.
The board (200 x 150 mm) is fully designed in-house: a PCB stackup of 18 layers was mandatory to connect all the external peripherals, in particular special care was taken for the DDR3 interface and the high speed links (impedance controlled differential pairs with equalised lengths).
A pre-series batch of four unit has been built: all the boards powered up correctly, and we started the debug phase, writing the necessary Verilog code to investigate the behaviour of the two most critical parts: the DDR3 RAM and the 10 Gb/s links. Both were successfully tested, the former with a 8 GB module running at 1333 MHz (Hard Memory Controller inside the FPGA), the latter with a low latency Ethernet MAC core plus custom logic that implements IP/UDP packet handling. At the moment an in-house developed custom FMC module has been plugged in the FMC LPC connector, thanks to which we are able to control and collect the data generated by a 16-bit, 125 MS/s four channel ADC (AD9653).





Key features:

- SODIMM connector for DDR3 RAM
- Gigabit Ethernet link (SGMII)
- 4 SFP+ modules up to 10 Gb/s
- real time clock (RTC) with backup battery
- Si5340 clock conditioner
- 40 GPIOs exported on connectors
- USB 3.0 interface
- socket for microSD card
- 2 FMC connectors, one HPC and one LPC



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FUTURE WORK

- Move to a System-on-Chip: hard processor (ARM) and FPGA in the same package
- Use this platform for testing in-house developed FMC modules
- Replacement of a complete microTCA Cavity BPM rack with the new boards