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# A COMMON DIAGNOSTIC PLATFORM FOR ELETTRA 2.0 AND FERMI

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*Abstract*

Elettra 2.0 is the project of upgrading the current synchrotron light source to a low emittance machine. In this framework, various components of diagnostics have to be refurbished due to the obsolescence of the same or due to the tight requirements of the new accelerator. In this paper we present a high performance FPGA-based (Altera/Intel Arria 10) digital board developed internally, capable of hosting two FMC modules, equipped with DDR3 ram and 10 Gb/s Ethernet links. The presence of the FMC connectors allows a flexible use of the board: various configurations of A/D and D/A converters (different number of channels, resolution, sampling rate) can be obtained, also with various I/O ports for trigger and synchronisation. These features make it applicable as a base platform for various applications not only for Elettra (electron and photon BPMs, DLLRF systems, etc.) but also for Fermi (cavity BPMs, bunch arrival monitor, link stabiliser). The peripherals on board have been fully debugged, and probably a new version with a SoC (System on Chip) will be released in the next future.

## INTRODUCTION

In a previous paper [1] we introduced a prototype of an electron Beam Position Monitoring system based on pilot-tone compensation, fully integrated in the Global Orbit Feedback system (GOF) of Elettra. In order to separate the analog and digital subsystems of the prototype, a modular design has been implemented. In this manner we had the chance to design, test and improve the analog signal conditioning subsystem, whose main goal was to feed any suitable digital acquisition system. The analog front end is still under testing even by external institutes, but up to now it has always shown remarkable performances [1]. For the first in-house evaluation of the front end, we put together a set of evaluation boards that globally acted as a digitiser; the drawback of this approach was the phasing out of various constituting devices, so they were not recommended for new designs. The evident lack of technology which was lived up to expectations, pushed us to develop in-house a suitable board with conversion and processing equipment powerful enough to be adopted as a generic board for a number of different diagnostics applications, both for Elettra 2.0 and Fermi accelerators. Taking into account that the operation of both accelerators relies on old equipment whose failure rate is supposed to increase over time, the design of this new generic board fulfils two goals: upgrade the full set of Elettra BPMs in the short time, replace the remaining acquisition systems in the long time.

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## DIGITAL PLATFORM FOR EBPM

The prototype is based on an Altera Stratix III FPGA, whose functional blocks are:

- two separate digital receivers (the first for beam signal, the second for the pilot tone) with CIC and FIR filters;
- two UDP Ethernet cores with SFP modules (Gigabit Ethernet);
- an external memory controller (1 GB of DDR2).

That design uses about 50 000 logic elements, 2 Mbit of embedded memory (FIFOs) and 88 DSP blocks. The incoming signals are digitised by four LTC2209 (16-bit, 160 MS/s), driven by a low jitter sampling clock synchronised with the machine clock of Elettra.

The new eBPMs, based on the incoming platform, should:

- house two complete BPM systems, optimising hardware, logic resources and interlock capabilities (angle detection);
- collect ADC raw data in a DDR SDRAM for post mortem and turn-by-turn beam analysis;
- share the acquired data by high speed links for reduced latency (10 Gbit/s);
- undersample the inputs by high-linearity 16-bit ADCs;
- drive the ADCs with a low jitter clock synchronised with the external reference (machine clock);
- export several digital I/Os (trigger, interlock, post mortem, ...);
- use four LTC2107 ADCs (16-bit, 210 MS/s). They have been already tested on an in-house developed FMC module and have shown better overall performances than the previously adopted LTC2209.

## REPLACING DIAGNOSTICS IN ELETTRA AND FERMI

Since their first operation (1993 Elettra, 2010 Fermi), both lightsources rely on various equipment fully developed and built in-house. Due to ageing, it is mandatory to service partially or totally the installed equipment; the list of the systems involved in diagnostics tasks that need to be refitted is reported below:

- Low-Level RF system (LLRF - Elettra): it controls phase and amplitude of the RF power applied to the cavities that maintain stable the energy of the beam;
- RF Cavities Monitor (Elettra): it monitors the operating parameters of the cavities (vacuum, reflected power, temperature) and generates an interlock whenever required;
- Beam Dump Monitor (Elettra): it is a distributed system that acquires a number of critical operating parameters at turn-by-turn data rate, such as RF cavities power, beam current, radiation, interlock system. These data are sampled with a common timebase, aimed to bet-

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ter understand the temporal sequence of beam dump events. Additionally, the system is capable to prevent superconducting cavity quenches originated by sudden beam loss caused, for example, by magnet power supply failure.

- Cavity Beam Position Monitor (C-BPMs - Fermi): it measures the electron beam position in the single pass free electron laser which repetition rate is up to 50 Hz. The calculated position has a resolution better than 1 µm adopting a self compensation strategy [2];
- Bunch Arrival Monitor (BAM - Fermi): it measures the arrival time of each bunch in specific sections of the accelerator in order to define a precise bunch timestamp [3];
- Link Stabilizer (LS - Fermi): in the timing distribution of Fermi, it measures the phase variation in the accelerating cavities with respect to a reference signal.

Even if the purposes of these systems are very different among them, they share several aspects from the electronics point of view: acquiring input signals (analog and/or digital), performing processing, transmitting data to the control system and, when required, generating local outputs (analog and/or digital). If the analog treatment of the signals and the AD/DA conversion tasks are detachable, a digital platform designed in a modular way can be shared among many different applications.

Furthermore, the modular approach is well-suited to Elettra and Fermi control systems topology that acquire data by distributed sensors and perform in a centralised server all the calculations required to drive the actuators in order to maintain stable the beams orbit. The Cavity BPMs, for example, send the acquired waveforms to the control system CPU over a standard Gigabit Ethernet link and not via the microTCA backplane, allowing physical separation between acquisition and calculation equipment even over long distances.

## OLD PLATFORM

In order to clearly show the advantages of the modular approach, we briefly describe the old platform (ADA/ADO) that is the core of the Cavity BPMs, the BAM and the LS systems (Figure 1). This microTCA device was developed in 2009 [4] to interface Fermi timing and diagnostics equipment to the machine control system. The architecture, as shown in Figure 2, is based on a Xilinx Virtex-5 FPGA (XC5VSX50T, 52 000 logic elements, 4.8 Mbit of embedded memory, 480 I/Os and 1136 pins) that handles all inputs and outputs on board, in particular the two SFP Gigabit Ethernet links and the 4 LTC2209 ADCs (for ADO, used in BAM) or the 2 LTC2209 ADCs and 2 MAX5890 DACs (for ADA, used in C-BPM). Unfortunately, the Virtex-5 has been discontinued, so the whole board has to be redesigned.

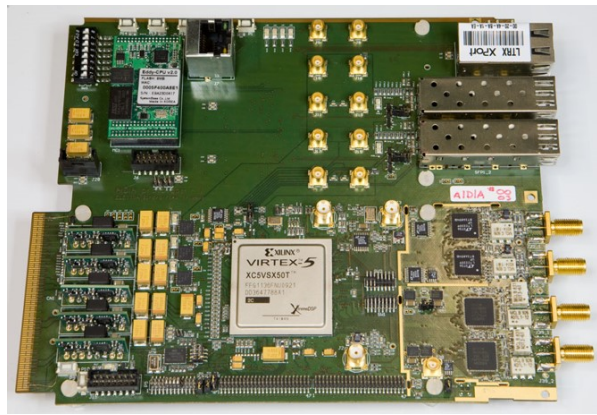


Figure 1: ADA board.

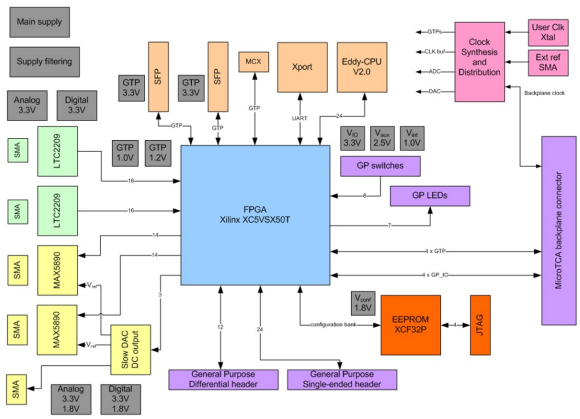


Figure 2: ADA board block diagram.

## NEW PLATFORM

Following the modular concept, we are developing a brand new platform called dgDAQ, whose core is an Altera/Intel Arria 10 570 GX FPGA, with:

- 570 000 LEs (logic elements);
- 868 000 registers;
- 3046 DSP blocks;
- 35 Mbit of embedded memory;
- 24 transceivers capable of 12.5 Gbit/s;
- 1152 pins with 222 LVDS pairs.

According to the previous "Digital platform for eBPM" paragraph, the following peripherals are connected to the FPGA (Figure 3):

- a SODIMM connector for DDR3 RAM;
- one Gigabit Ethernet link (SGMII);
- 4 SFP+ modules up to 10 Gb/s;
- a real time clock (RTC) with backup battery;
- a Si5340 clock conditioner;
- 40 GPIOs accessible by dedicated connectors;
- an USB 3.0 interface;
- a socket for microSD card;
- 2 FMC connectors, one HPC and one LPC.

The FMC connectors are the key feature that gives the demanded flexibility: in fact the specific final configuration of the system essentially depends on the installed FMC module.

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For example, in the dual eBPM case, two FMC modules with 4 ADCs are necessary, whereas for dual Cavity BPMs, two FMC modules with 2 ADCs and 2 DACs are to be mounted.

The board (200 x 150 mm) is fully designed in-house: a PCB stackup of 18 layers was mandatory to connect all the external peripherals, in particular special care was taken for the DDR3 interface and the high speed links (impedance controlled differential pairs with equalised lengths).

A pre-series batch of four unit has been built (Figure 4): all the boards powered up correctly, and we started the debug phase, writing the necessary Verilog code to investigate the behaviour of the two most critical parts: the DDR3 RAM and the 10 Gb/s links. Both were successfully tested, the former with a 8 GB module running at 1333 MHz (Hard Memory Controller inside the FPGA), the latter with a low latency Ethernet MAC core plus custom logic that implements IP/UDP packet handling. At the moment an in-house developed custom FMC module has been plugged in the FMC LPC connector as shown in Figure 5, thanks to which we are able to control and collect the data generated by a 16-bit, 125 MS/s four channel ADC (AD9653).

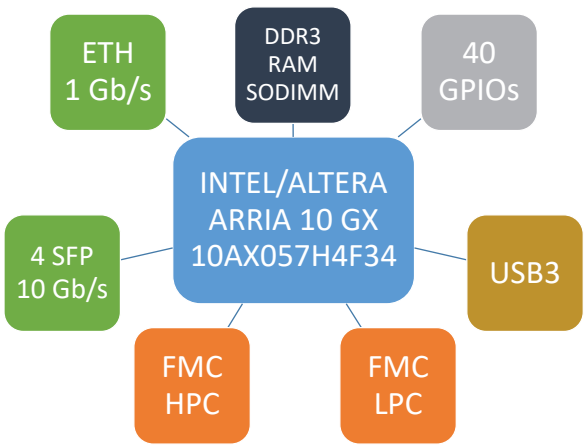


Figure 3: Arria 10 dgDAQ board block diagram.

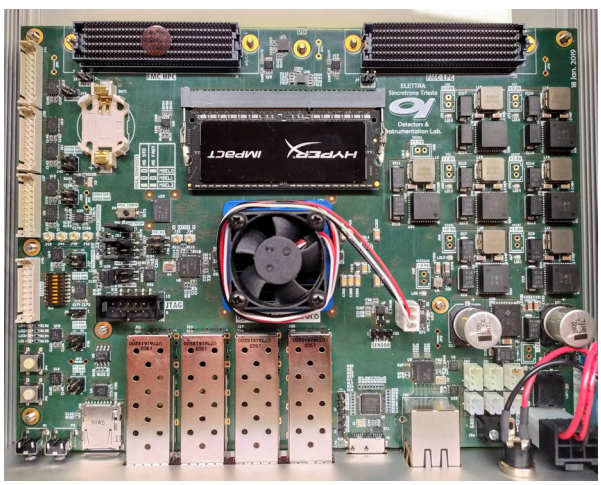

Figure 4: Arria 10 dgDAQ board.

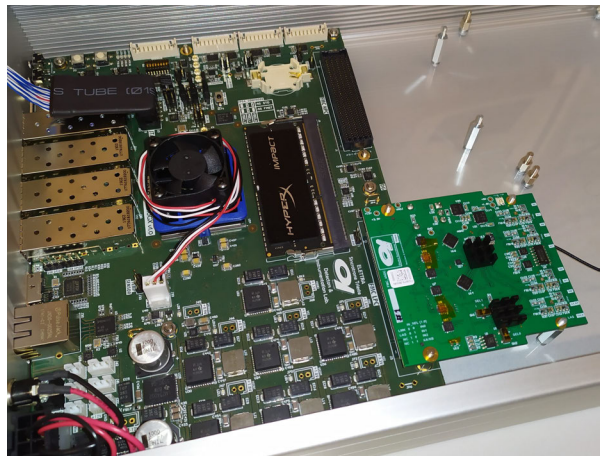

Figure 5: Arria 10 dgDAQ board with FMC module.

## CONCLUSION

The development of an in-house designed FPGA-based platform has been presented and first excellent results have been exposed, showing very good performances in treating high-speed signals. As a next step, we will use this platform as a test bench for the in-house developed FMC modules. Only after the development and test of an appropriate number of modules we will start replacing the old diagnostics electronics. However, fundamental upgrades are planned, and one of the most meaningful consists in moving towards a System-on-Chip of the same family (Arria 10 SX). This architecture provides a physical ARM processor (HPS, hard processor system) linked with the FPGA in the same package. The presence of a physical CPU will simplify in particular the system maintenance for high-level tasks: remote firmware upgrade of the FPGA, configuration and communication via SSH, presence of TANGO server on board are useful features that will be easily implemented through a resident operating system.

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