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DIRECT-SAMPLING COARSE BUNCH ARRIVAL TIME MONITOR IN THE FREE ELECTRON LASER FLASH BASED ON THE FAST DIGITIZER IMPLEMENTED IN THE FMC VITA 57.1 STANDARD

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Abstract

At the free-electron lasers FLASH and European-XFEL bunch arrival times are monitored with a high-accuracy electro-optical based data acquisition system (BAM). Due to only a couple of picoseconds time measurement range of this system, large timing changes might cause the monitor to fail. To remove any ambiguity and for health status monitoring a high-speed direct-sampling FPGA mezzanine card (FMC) and an analogue RF front-end was added. The circuitry has lower precision than the electro-optical based BAM, but it can determine bunch arrival time with respect to a reference signal over a large time range, i.e. of the order of 1 ms. After restarts or larger energy changes during operation, the electron bunch arrival time may have been changed by tens or even hundreds of picoseconds, which causes that the BAM is out of its operation range and needs to be recalibrated. With the solution developed, the BAM gets the coarse bunch timing from the digitizer and adjusts its optical delay lines accordingly. This allows for finding the operation point fast and automatically. Performance data of the fast direct-sampling digitizer FMC and first measurement data from FLASH will be presented.

INTRODUCTION

In modern linear accelerators like *Free-Electron-Laser in Hamburg* (FLASH) or the *European X-Ray Free Electron Laser* (E-XFEL) one of the most critical systems is the *Low-Level-RF* (LLRF) control system. In FLASH and E-XFEL these systems are realized using the *Micro Telecommunication Computing Architecture* (MTCA.4). For measuring the pick-up signals coming from the accelerating superconducting cavities, a mixer is used to convert the 1.3 GHz signals down. Down converted signals are then fed into a digitizer. For several diagnostic applications like coarse *Bunch Arrival Time Monitor* (BAM) [1–3] or *Higher Order Mode* (HOM) sampling a cheaper and more simple solution is needed.

The mixer approach needs a very stable and accurate *local oscillator* (LO) signal, which generation can be expensive. To overcome this disadvantage, a direct-sampling digitizer based on an ADC with up to 1 GS/s was developed at DESY in 2018. First prototypes was tested and the second revision is in development right now. Figure 1b shows the first revision of the digitizer in ANSI/VITA 57.1 2010 FMC form factor. BAM and HOM are realized as first test applications to see if the board can achieve the desired performance.

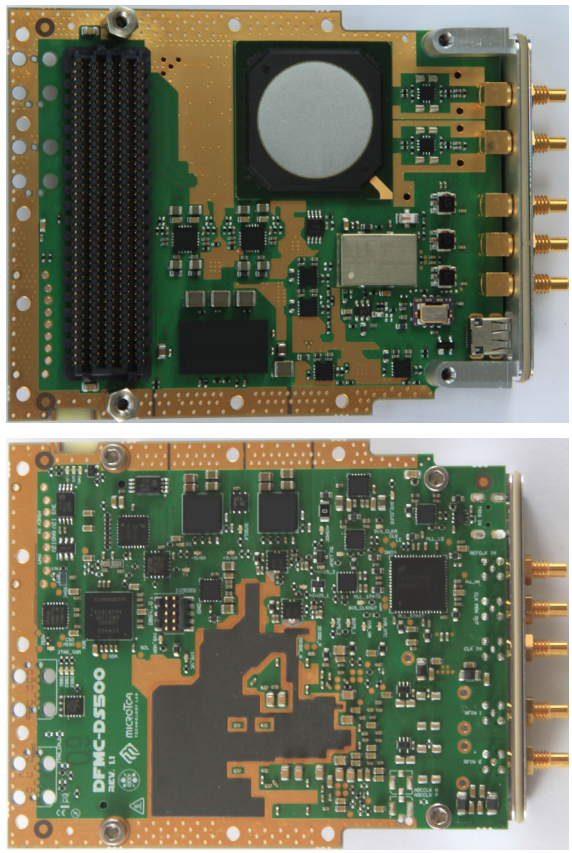

Figure 1: DFMC-DS500 digitizer board (a) top view (b) bottom view.

The new digitizer can be easily integrated in the existing MTCA infrastructure and is used in combination with the DESY *Advanced Mezzanine Card* DAMC-FMC25 FMC carrier board .

THEORETICAL ESTIMATION OF DIGITIZER PERFORMANCE

Before starting to measure the performance of the board a rough estimation of the resolution and SNR can be done. The frequency of the BAM and HOM signals is well known and always above 1 GHz. The BAM front-end has a bandpass filter with f_c = 2.38 GHz. The digitizers SNR and aperture

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jitter are the most critical parameters to achieve the desired accuracy. If one assume a clean sinusoidal input signal to the ADC, SNR can be calculated using:

$$\mathrm{SNR} = -20 \cdot \log_{10}(2 \cdot \pi \cdot f_{in} \cdot t_j), \quad (1)$$

with t_j the combined aperture and clock jitter

$$t_j = \sqrt{{t_{aj}}^2 + {t_{cj}}^2}. \quad (2)$$

Equation (1) assumes an infinite resolution ADC. Aperture and clock jitter is the only factor in determining the SNR [4–6]. For the used ADC the aperture jitter can be found in the data sheet and is $t_{aj} = 200fs$. This value is fixed and cannot be changed.

Second limiting factor for the ADC performance is the *Noise Spectral Density* (NSD). On the DS500 a 12-bit ADC with a sampling rate of 500 MS/s is used, thus the SNR over the full nyquist range of an ideal ADC is:

$$\mathrm{SNR} = 6.02 \cdot 12 + 1.76\ \mathrm{dB} = 74.04\mathrm{dB}\ [7].$$

Noise is spread across a 250 MHz nyquist zone and the noise per 1 Hz is calculated with:

$$\begin{aligned}\text{Noise power per bin} &= -10 \cdot \log_{10}(fs/2) \\ &= -83.98\ \mathrm{dBFS/Hz}.\end{aligned}$$

The ADC is not an ideal ADC and the NSD can be found in the data sheet and is −149.6 dBFS/Hz. With this value one can estimate the SNR of the used ADC which is:

$$\begin{aligned}\mathrm{SNR} &= -\mathrm{NSD} - \text{Noise power per bin} \\ &= -149.6 + 83.98 = -65.62\ \mathrm{dB}\ [8].\end{aligned}$$

With Eq. (1) and the estimated SNR of the ADC, clock-jitter limited SNR can now be plotted over input frequency [6, 8]. Figure 2 depicts the SNR degradation for four different clock jitter profiles t_{cj} ranging from 10 fs to 300 fs. The black lines are calculated using Eq. (1) and the combined jitter is calculated using Eq. (2). One can also see the red line which is the approximated SNR depending on the NSD of the used ADC at a sampling frequency of 500 MS/s. The magenta and green curves are the SNR and SINAD extracted from the data sheet [9]. It is clearly visible that from a certain input signal frequency, where the red line crosses the black curves, the combined aperture and clock jitter dominate the SNR degradation. The higher the sampling clock jitter the lower the input frequency where jitter degradation starts. With degradation of SNR the *effective number of bits* (ENOB) gets lower and ADC resolution is decreased.

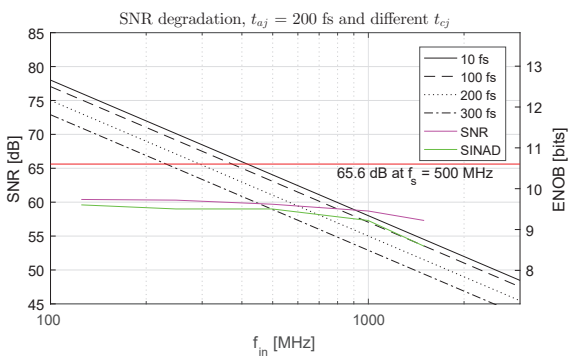

Figure 2: SNR degradation for clock jitter values t_{cj}.

As stated above the input signals for BAM measurements are above 1 GHz. In this frequency range only the clock jitter impairs SNR and SINAD. Comparing the theoretical estimated performance of the ADC with the values extracted from the data sheet clarifies that the estimation for input frequencies lower then the sampling frequency is better then the achievable performance. The ADC is significantly worse. The theoretical estimation of the NSD dependant SNR do not take the distortions and thermal noise [10] of the ADC into account. In the higher frequency range the degradation of ENOB and SNR is obvious. Even if the sampling clock is jitter free, the internal aperture jitter of 200 fs [9] degrades SNR and ENOB for input signal frequencies above 500 MHz. The green curve is the SINAD of the ADC and this curve fits very well to the estimated degradation of SNR. The SINAD includes distortions caused by clock jitter.

Sampling clock jitter is the most important parameter to optimize if undersampling of high frequency signals is needed and not to degrade the inherent performance of the ADC itself.

IMPROVEMENT OF FMC DIGITIZER DFMC-DS500

The key component on the DFMC-DS500 is the 12-bit, 500 MS/s dual-channel ADC12D500RF from Texas Instruments [9].

It can be operated in single-channel mode (non-DES) or in *dual edge sampling mode* (DES). In DES mode the signal is presented to both input channels of the ADC through an internal multiplexer or external components. During DES mode operation the sampling clock of one channel is shifted by 180°. The −3 dB input bandwidth in non-DES and DESCLKIQ mode is 2.7 GHz. In DESI, DESQ and DESIQ mode input bandwidth is reduced to 1.2 GHz [9].

Figure 3 shows the improved block diagram of the second revision of the board. Major changes affect the power management to solve power sequencing and monitoring issues. Minor changes were made in the power supply section to improve noise especially for the PLL and the loop filters. The front panel interface via the MicroHDMI connector is now capable of providing 12 V or 3.3 V. This simplifies development and control of custom made analog front-end electronics. An input attenuator and a noise filter are added to the *fully differential amplifier* (FDA) stage as well as a frequency compensation network to flatten the frequency response [11].

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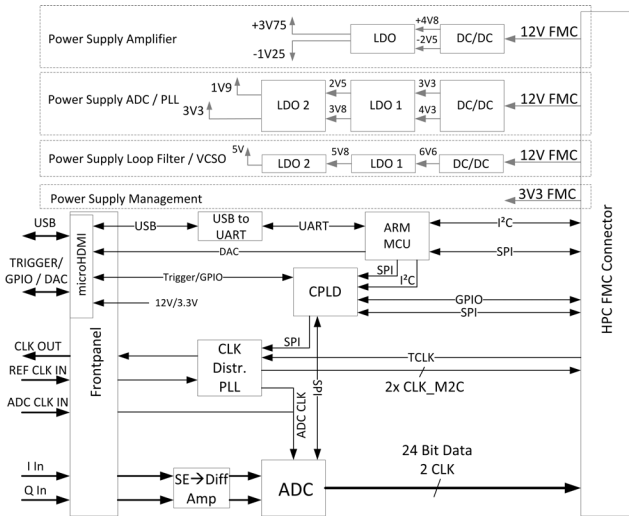

Figure 3: Block diagram of the DFMC-DS500 digitizer.

Clock Tree

As stated in the section before care should be taken by generating a low jitter sampling clock. Thus, the on-board *phase locked loop* (PLL) is changed in the new revision of the board. The actual PLL (120 fs) will be exchanged to achieve a minimum clock jitter of around 60 fs. Dual loop operation allows to jitter clean the *telecommunication clock* (TCLK) provided via MTCA back plane by the carrier or any other reference clock.

ADC Performance Measurement Setup

In Ref. [12] the digitizers timing precision was measured using a 1.3 GHz DRO and an external divider to drive the reference input of the on-board PLL. The required accuracy of 1 ps was met but the result was not outstanding. Measurements made in Ref. [12] has shown that the PLL needs to be improved for undersampling the BAM signals.

To estimate the degradation of the ADC due to single-ended to differential converting amplifiers and PCB layout an improved measurement set up was developed.

Instead of using a DRO and a divider to drive the PLL input, an SMA100B signal generator with ultra-low phase noise and clock synthesizer option from R&S was used to drive the ADC clock input directly. The clock and the RF output of this generator have an integrated jitter of 18 fs from 10 Hz to 20 MHz beside the carrier.

With this setup the timing error was measured again. A 2.5 GHz output signal and a phase synchronous clock signal with a frequency of 500 MHz were generated leading to a sampled DC signal. The input signal to the ADC should drive its full scale range. Adjusting the DC signal to zero by tuning the phase shifter one can calculate the timing error. An overall timing error of 208 fs RMS was measured.

With the same setup an input signal with a frequency of 498 MHz was generated and sampled with 500 MS/s to compare the spectral response to the data sheet of the ADC [9].

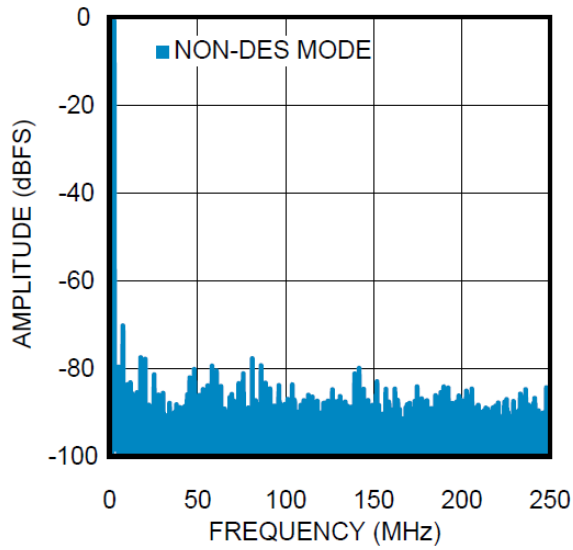

Figure 4: Spectral response extracted from [9], f_{in} = 498 MHz.

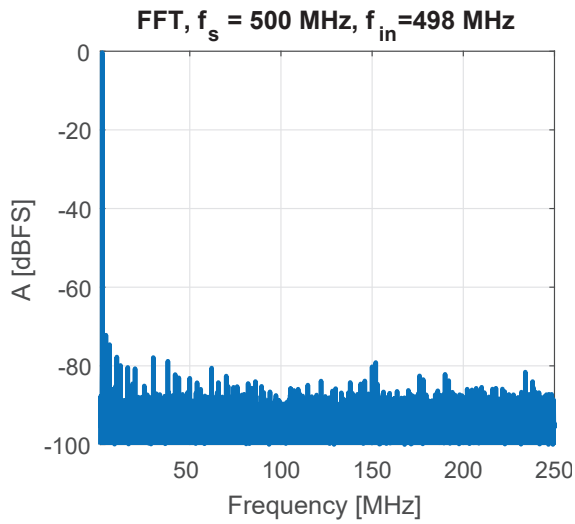

Figure 5: Measured spectral response of DFMC-DS500.

Figures 4 and 5 show the spectral responses from the ADC data sheet and measured with the DFMC-DS500. The spurs produced by the DFMC-DS500 are a few dB higher due to the distortions produced by the input amplifiers.

COARSE RF BAM CHANNEL

An electro-optical BAM is operated in FLASH and E-XFEL accelerators to estimate bunch arrival time. The accuracy of this system is in the range of a few femtoseconds [2, 13]. The electro-optical BAM uses electro-optical modulators to modulate optical pulses with the electrical signal from the beam pick ups. To automatically adjust the optical delay lines of the BAM a second coarse BAM system was planned in FLASH. It measures the bunch arrival time with picosecond accuracy and provide the arrival time to the BAM.

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Beam Pick Up

The beam pick up in FLASH produces four broadband signals of which two opposite signals are combined together to reduce dependency to the transversal position of the beam. Then a coupler splits the signal into two. One of the signals is provided to the electro-optical BAM and the other to the coarse RF BAM channel.

The expected waveform from the pick ups can be approximated using a gaussian monocycle. Figure 6 shows two simulated monocycles for two different bunch charges (BC). The amplitude depends on the bunch charge and reaches for $BC = 200$ pC 40 V peak to peak. The highest power density for a cycle with $\sigma = 10$ps is located at 20 GHz but σ can vary from 5 ps to 10 ps which leads to high power densities between 20 GHz and 40 GHz [2].

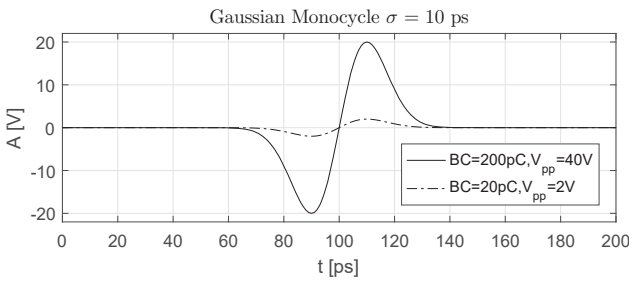

Figure 6: Simulated Gaussian Monocycles.

Analog Front End

To sample the broadband signal produced by the pick up the signal frequency has to be reduced. Figure 7 shows the implemented analog front end. In Figure 8 the analog signal processing chain is depicted. Due to varying bunch charges the amplitude of the signal can be as high as 20 V peak-to-peak which cannot sampled directly by the digitizer.

Thus, in the first stage the signal is attenuated by 5 dB and filtered by a low pass with a cut-off frequency of 2.75 GHz.

Figure 7: Coarse BAM analog front end.

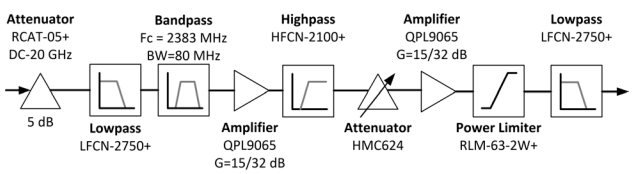

Figure 8: Block diagram of coarse BAM analog front end.

In the next stage a bandpass filter is used to further reduce signal frequency and to band limit the output signal to 80 MHz.

Between two variable gain amplifiers there is a highpass filter and a step attenuator. The highpass and the attenuator should prevent the two amplifiers to start oscillating. The attenuator can also be used to adjust the signal amplitude for driving the full scale range of the digitizer. The power limiter is very important in order to protect the ADC against excessive overloading. At the end of the chain there is a second lowpass with a cut-off frequency of 2.75 GHz.

Figure 9 depicts the first measured signal in the accelerator. This is the sampled pulse response of the AFE produced by the beam pick ups in FLASH.

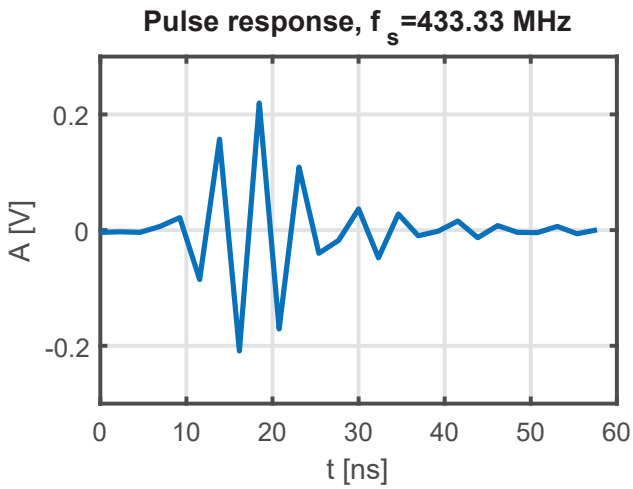

Figure 9: BAM pulse sampled in FLASH.

CONCLUSION AND OUTLOOK

The ADC performance degradation due to the single-ended to differential converting amplifiers and board layout is minimal. There are no large spurs visible. To minimize timing errors measured in Ref. [12] the PLL must be improved. The coarse BAM channel is installed in FLASH and can take samples. Next, the phase and bunch arrival time extraction from the sampled values needs to be implemented. After the arrival time can be extracted from the signal an algorithm to automatically adjust the delay line of the electro-optical BAM will be implemented and tested in FLASH.

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