PRELIMINARY DESIGN OF Mu2E SPILL REGULATION SYSTEM (SRS)

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Abstract

Direct μ→e conversion requires resonant extraction of a stream of pulsed beam, comprised of short micro-bunches (pulses) from the Delivery ring (DR) to the Mu2e target. Experimental needs and radiation protection apply strict requirements on the beam quality control and regulation of the spill. The objective of the Spill Regulation System (SRS) is to maintain the intensity uniformity of a stream of ~25k pulses as 1e12 protons are extracted at 590.08 kHz over a 43 ms spill period. To meet the specified performance, two regulation elements will be driven simultaneously: a family of three zero-harmonic quadrupoles (tune ramp quads) and a RF Knock-Out (RFKO) system. The SRS will use two separate control loops to control each regulation element simultaneously. It will be critical to coordinate the SRS processes within the machine cycle and within each spill interval. The SRS has been designed to have a total Gain-Bandwidth product of 10 kHz, which can be used to mitigate several sources of ripple in the spill profile.

OVERVIEW

The former Antiproton Source transport lines and storage rings have been upgraded and repurposed into the "Muon Campus" (Fig. 1) for experiments, such as g-2 and Mu2e.
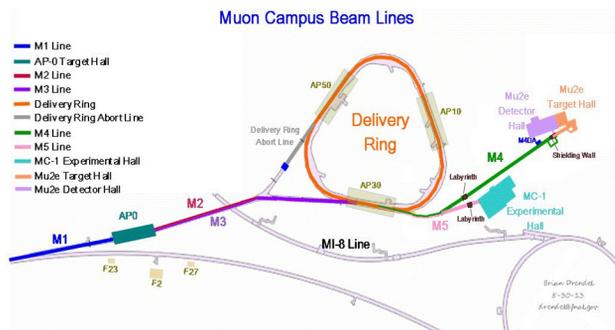

Figure 1: Muon Campus Map.

Mu2e proposes to measure the ratio of the rate of the neutrino-less, coherent conversion of muons into electrons in the field of a nucleus, relative to the rate of ordinary muon capture on the nucleus. This requires the resonant extraction of a stream of pulsed beam, comprised of short micro-bunches (pulses) from the Delivery Ring (DR) to the Mu2e target. Experimental needs and radiation protection apply strict requirements on the beam quality control and regulation of the spill [1].

Accelerator Timeline for Mu2E Proton Delivery

Depicted in Fig. 2, Mu2e uses 8 kW of 8 GeV protons from the Booster. Two batches of ~4e12 protons are sent to the Recycler (RR). In the RR, the beam circulates and is then re-bunched by a 2.5 MHz RF system. The batch is divided into 8 2.5 MHz bunches. Extracted at MI-52 from RR, the reformatted bunches are transported to the DR via P1, P2, M1, and M3 beam transfer lines.

Once 1e12 protons are injected into the DR, beam is then slow extracted to the Muon proton target at the DR revolution frequency of 590.08 kHz over a 43.1 ms spill period. Between each spill period, there is 5 ms reset period, in which there is no extraction. After the 8th spill, there is no beam in DR for 1.02 s. Dividing the total spill time by the length of the cycle, the spill duty factor is 27.1% [2].
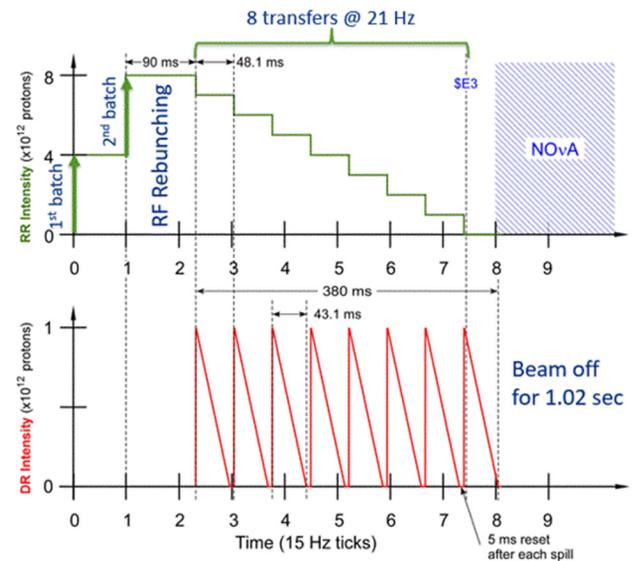

Figure 2: Mu2E Timeline.

Resonant Extraction in DR

By exciting 2 families of the harmonic sextupoles in the DR, the third integer resonant extraction condition is established [3]. Then, a family of 3 zero-harmonic quadrupoles (tune ramp quads) drives the machine tune to the exact resonance, gradually pushing the circulating beam into the resonance stop band. As unstable particles in the stop band drift towards the machine aperture, they get intercepted in the Electrostatic Septum (ESS) and are deflected towards the Mu2e target at the end of the extraction beam line.

SRS REQUIREMENTS

The SRS's objective is to maintain the intensity uniformity of the stream of ~25k extracted pulses from the DR

to the Mu2E target. Experimental needs and Radiation protection apply strict requirements on the beam quality control and regulation.

The maximum spill variation is required to be <±50%, while maintaining the extraction efficiency at >98%. At the end of the spill, there should be <5e10 protons left in the DR at abort.

The SRS will regulate extraction through 2 primary elements: a family of three zero-harmonic quadrupoles (tune ramp quads) and a RF Knock-Out (RFKO) system, using a power amplifier and a stripline kicker. Each regulation element is controlled by separate but synchronous feedback loops. The SRS has been designed to have a total Gain-Bandwidth product of 10 kHz, which can be used to mitigate several sources of ripple in the spill profile.

SRS INPUT SIGNALS

Spill Monitoring Signals

The SRS requires at least one spill monitor that can resolve on average ~4e7 protons at 10 kHz. Two options are a Wall Current Monitor (WCM) and an Extinction Monitor (EM). They can be used individually or in combination with each other. If needed, the SRS will provide dedicated optical links to the spill monitor(s), using a point-to-point protocol with basic error handling. If the latency of the signal acquisition from the spill monitor(s) is >1 ms, a timestamp is also required.

Clock Signals

The SRS will use the 18.86 MHz clock from the Muon LLRF system to derive clocks for signal acquisition, data processing, and signal generation. Any derived clocks will be phase-locked to the LLRF and will reset anytime the LLRF turns off during RF manipulations.

Timing Signals

The SRS will need to decode predefined machine TCLK and Beam Sync (BS) timeline events. This will enable the SRS to coordinate its processes with accelerator operations.

Additionally, the SRS requires the Muon campus turn marker, which will be aligned with the bucket 0 of the DR. Counting the turn marker allows the SRS's processes to remain synchronized with the accelerator timeline during the cycle.

In addition, SRS must be able to acquire timing signals on both single- and multi- mode optical fiber links, with it installed as part of the Muon campus timing infrastructure.

TUNE QUAD MAGNET REGULATION

The main way to control the extraction is by regulating the reference to the tune ramp quads. The SRS will control a family of 3 tune ramp quads.

Each magnet is a CQA type from electron cooling ring [4]. Each one is located at the center of each of the three straight sections for the slow extraction from the DR. Their bandwidth is limited by the magnet inductance and by the

corner frequency introduced by the field propagation through the stainless beam pipe.

Because of the location of these three magnets, it is planned to drive each magnet with a separate supply. Each magnet has two 65 A switching power supplies (PS) in parallel, making a 160–180 V switcher with 130 A, maximum. Each power supply will supply 8 status bits, while the PS controller will have an additional 8 status bits. These status bits can be monitored by the SRS, for fault protection.

In addition, the supplies of the tune quads will be daisy-chained, and their reference ramp curve will be generated by the SRS. This reference determines the average shape of the beam intensity profile during the spill. The quadrupole ramp has a maximum dI/dT of 16,000 A/sec, with nominal current of 80 A.
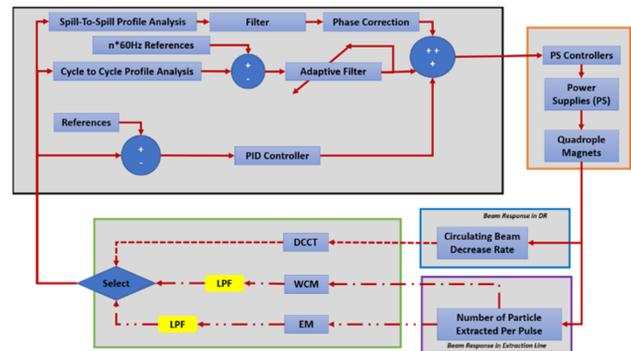

Figure 3: Tune Quad Control Loop.

During a 5 ms reset period in between spills, the SRS will ramp the tune-ramp quads to near the extraction resonant.

Once beam is injected, the SRS's Tune Quad Control Loop (Fig. 3) will immediately regulate the ramping curve, keeping the spill out of the DR linear. The processing within the feedback loop consists of 3 main elements: PID controller, an adaptive filter to cancel 60Hz harmonics within the cycle, and a spill-to-spill filter to be applied with phase correction.

During the 1.02 s no-beam time, the SRS will drive magnets to a pre-determined low power pedestal.

RFKO REGULATION

Using a solid-state power amplifier and a stripline kicker, the RFKO system is used to fine tune the extraction rate and spill profile, by heating the beam in the horizontal plane, accelerating the diffusion of particles.

RFKO Stripline Kicker

A 1.4 m stripline kicker, previously used as a Tevatron damper kicker, will be used to provide 1 uRad single pass kick @ 1 kW power.

The SRS will generate the RFKO's FM excitation signal, whose carrier frequency is tracking the current betatron sideband. The SRS will calculate this from the spill profile provided by the Tune Quad Control Loop. The excitation signal can either be a sweep modulation (ex. chirp) or "colored" noise.

Furthermore, the SRS's RFKO Control Loop (Fig. 4) will regulate the amplitude of this excitation signal. The processing within the feedback loop consists of 2 main elements: a PID controller and a spill-to-spill filter to be applied with phase correction. During reset and no-beam periods, the control loop will be disabled.
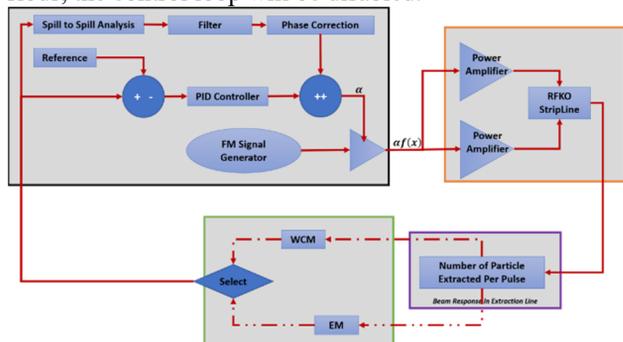
Figure 4: RFKO Control Loop.

The amplitude-regulated excitation signal is applied to each of the stripline's plates, which will be terminated with a high power 50Ohm terminator.

The resulting RF horizontal kick excites the beam at the betatron frequency and causes the beam to heat transversely. The diffusion of particles into the stop band accelerates, allowing particles to transition though the separatrix and "spill out" into the unstable region. Emittance growth occurs only horizontally at a rate of 0.6e-3 m/sec at 500 W.

SYSTEM ARCHITECTURE

The SRS architecture will be based on the controller board for Mu2e LLRF system [5]. It consists of the System-On-Module (SoM) and a carrier board. The SoM is a FPGA mezzanine card that hosts the Intel Arria10 SoC. As shown in Fig. 5, the SoM uses bottom FMC connectors that mount onto a carrier board, which is mounted in a rack-wide chassis. The FMC connectors provide two PCIe x8 Gen3 LVDS lanes, to interface with the components on the carrier board. The carrier board hosts the peripherals, including but not limited to a clock distribution chip, ADCs, and DACs.
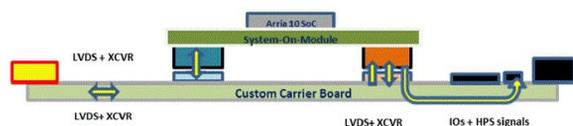
Figure 5: Side view of mounted SOM on carrier board.

Carrier Board

The carrier board (Fig. 6) provides 16 ADC channels, each with 16-bit resolution and 650MHz input bandwidth. These channels can be configured to be either DC-coupled or AC-coupled.

Also, the board provides 8 high speed 14bit DAC channels. Each DAC channel shall support update rates up to 125 MSPS. All high-speed DAC channels shall be capable of being AC or DC coupled with minimal modifications to the board.

Additionally, the board has 4 DAC channels with a 16-bit resolution and a slower sample rate of 200 kSPS. The data to the DAC is transferred from the SoM through an independent SPI port running at a clock rate up to 25 MHz. These outputs must be differentially coupled with a 5 Vpp maximum swing.

The board also has 8 TTL level tolerant Schmidt trigger inputs. Two of these inputs are used to acquire the timing signals for decoding machine events and machine data. The decoding logic shall be provided in SoM.

The board also has16 TTL level, 50 Ω drive capable digital outputs, connected to a coax connector on the front panel. These can be configured for diagnostic signals or control signals to external systems, such as the Machine Protection System (MPS).
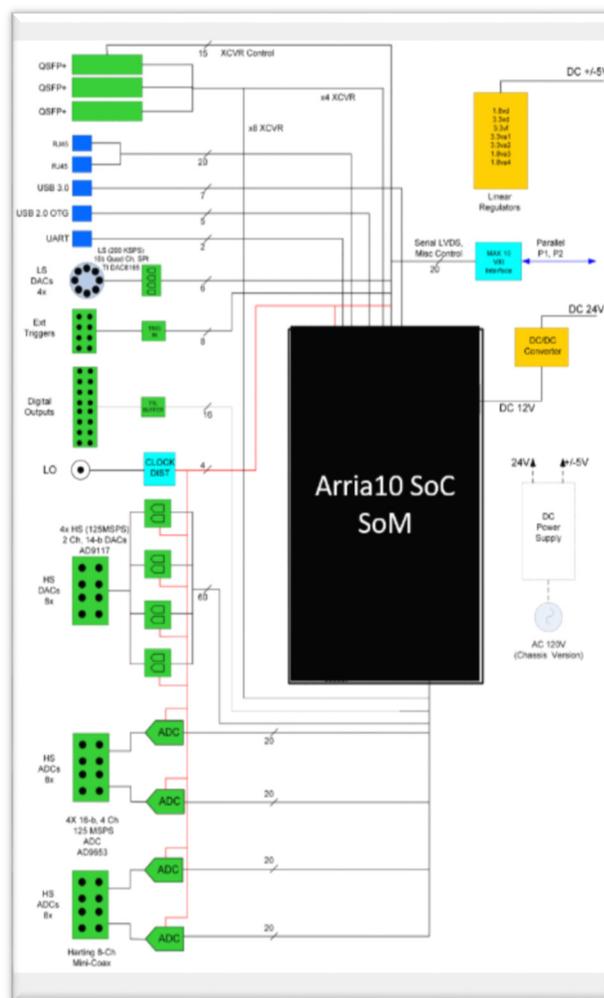
Figure 6: Carrier Board.

Arria10 SoC SoM Board

The SoM board provide a real-time clock, a programmable clock generator, DDR4 memory, MAX10 CPLD, and the Arria10 SoC FPGA. Both the SRS's firmware and front-end software will be implemented on the SoM FPGA (Fig. 7).
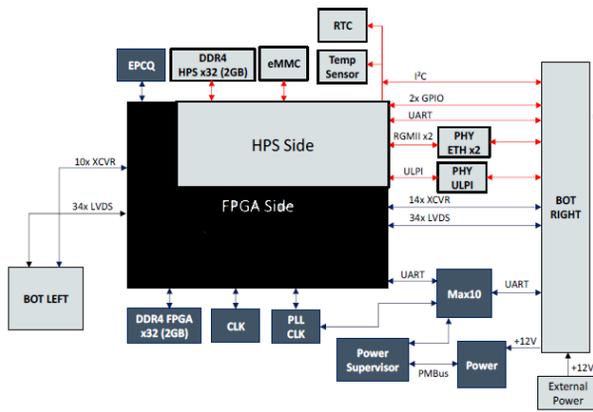
Figure 7: SoM Block Diagram.

Arria10 SoC features a second-generation dual-core ARM Cortex-A9 MPCore processor-based hard processor system (HPS). Upon power-up, the Arria10 FPGA automatically loads via a quad serial interface with a dedicated FLASH EPCQ in active serial configuration mode. Then, HPS boots from on-chip ROM in the FPGA, which initializes all required hardware components and fetches the bootloader binary. The bootloader is responsible for loading the Linux kernel and its device tree as well as mounting the root file system. Within the Linux OS environment, each core acts on a single thread of execution, which is interruptible to service different requests.

One ARM Core will be designated for the front-end software application which provides an interface between the FPGA controller and the ACNET control system. Its tasks include, but are not limited to, mapping system memory, initializing system parameters, and servicing connection and data requests from the ACNET control system and diagnostic tools, such as Labview.

Additionally, the second ARM core of the HPS can be dedicated to calculating cycle-to-cycle feedforward corrections. The HPS will access buffers captured during the previous n-spills. The data will be analysed during the 1.02 s no-beam period to update feedforward parameters as well as optimize the ramping curves and reference signals for the future cycles.

The HPS and FPGA fabric will be interconnected thru the Platform Designer (formerly Qsys). In effect, firmware modules, including NIOSII soft processors, are viewed by the HPS as peripherals. Each module in the FPGA portion of the SoC can operate concurrently and synchronous to the phase-locked clocks (Fig. 8).

The data acquisition system (DAQ) is implemented in the FPGA fabric. The DAQ includes ADC receiver blocks to decode a serial stream from 2 x 8-channel ADC's for a total of 16 ADC channel inputs and a DAC transmitter block to convert 8 channels of 66 MHz data to 4 x 2-channel DAC's. The DAQ system is capable of sampling two signals at full speed of 66 MHz to fill up to 1 GBytes of memory (1.9 s).

In addition, the FPGA instantiates multiple NIOSII 32-bit embedded processors. One configures and controls the modular scatter-gather DMA engines. It also handles DAQ operating mode changes, controls the FPGA sample and

serializer block, and handles 'buffer full' interrupt signals to the ARM.

The other 2 serve as floating-point processors for the regulation controller loops. Each of the control loops are standard PID controllers applied to a discrete closed loop control. After computing the difference between a reference and an input signal, every part of the PID contributes to a specific action. The proportional stage drives the controller output according to the size of the error. The integral stage eliminates the state-steady offset. The derivative stage evaluates the trend to correct the output and improve overall stability by limiting overshoot. The result of each stage is combined to create a fast responding but stable system.
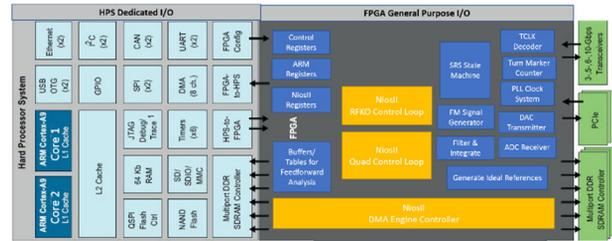

Figure 8: Block Diagram of Firmware.

CONCLUSION

This short document describes the preliminary design of the Mu2E Spill Regulation System. Phased implementation is currently underway. The commissioning of the beam line with single turn extraction in fall of 2020. Slow extraction is planned to start during commissioning in FY2021.

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