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DEVELOPMENT OF NEW LOSS MONITOR ELECTRONICS FOR THE HIPA FACILITY

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Abstract

A replacement for the ageing electronics of loss monitors at HIPA is under development. We discuss requirements, concepts and first tests of a prototype.

INTRODUCTION

Some 320 signal currents from ionization chambers, collimators, aperture foils, halo monitors and beam stoppers in the HIPA facility [1] are read out by several types of in-house developed CAMAC modules, which also generate interlocks to protect the machine from irregular beam. Most types are based on logarithmic amplifiers to cover the large dynamic range of signals. After 20 to 35 years of operation, the electronics approaches the end of its life cycle. With a limited number of spares, discontinued components, outdated standards, incomplete documentation and the system specialists all retired, maintenance gets increasingly difficult. At the same time the risk of causing significant downtime increases, since nearly all supported devices are, other than, e.g., profile monitors, essential for machine protection in normal operation. The need for a replacement of the ~190 involved CAMAC modules, including high voltage (HV) supplies for the ionization chambers (IC), is evident. However, with limited resources, it is still under discussion when it should take place.

We started a pre-project to evaluate a modern version of a logarithmic amplifier in combination with a system-on-module data processing unit and state of the art network connectivity. A single type of module should provide the needed wide current range, speed, computing capability and connectivity. Making use of modern technology capabilities, we intend to implement several improvements of the electronic functionalities [2]:

1. Refined rules for interlock generation to allow safe operation with fewer restrictions to operation.
2. Capability for checking the performance of detectors, cables and electronics when beam is switched off.
3. Storage of data series for post-interlock analysis and other studies.

In the long term, the new module can also be a part of the replacement of the remaining 36 CAMAC modules for the control of wire monitors and beam-induced fluorescence monitors.

REQUIREMENTS

Amplifier

Signal currents from the diagnostic devices, mostly loss monitors, are permanently measured and evaluated. ICs as well as collimators and secondary emission foils all deliver positive currents, which need to be measured in the range of 20 pA to 20 mA.

A bandwidth of 50 kHz allows to switch off the beam fast enough to prevent thermal damage to accelerator components in case of accidental loss of the full and even focused beam. This is needed above 10 nA where the interlock levels are usually set. This bandwidth is also sufficient to resolve an, e.g., 40 µs long beam pulse when pulsing the 870 keV beam line with 500 Hz for test purposes. Also the effects of the 7 ms long pilot pulses preceding the switching of the full beam to the ultra-cold neutron source [3], as well as conceivable, even shorter, single 'explorative pulses' for the study of new beam optics [4], are resolved.

With logarithmic amplifiers, care has to be taken to prevent latch-up from short negative current spikes, which are part of AC electromagnetic interference, which may cause a delayed response to following positive currents. Here a low-pass filtering and the permanent injection of a bias current of, e.g., +100 pA are helpful. Any hardware filters must be applied before the logarithmic amplifier to conserve average values.

To prevent ground loops, the amplifier ground is separated from rack ground (Fig. 1, a high impedance Z1 is required). The individual ground for each channel is provided via the shield of the long signal cable to the detector [5-7].

Bias Voltage

A voltage source applied between amplifier ground and the shield of the long cable, allows to bring the amplifier, and with it the connected collimator or secondary emission foil, to a bias potential (Fig. 1). This can be used for several purposes [2]:

1. Isolation check of collimator and cable, measured without beam (negative voltage).
2. Suppression of secondary electrons from collimators to get a more accurate reading of the stopped beam current fraction, especially in the 870 keV beam line and the first turns of the Injector 2 cyclotron, where the secondary electron yield is >1 (positive voltage).
3. As a side effect, in the 870 keV line, this may lower the degree of local space-charge compensation. The impact on beam emittance has to be evaluated.
4. Suppression of thermionic electrons from wire monitors and radial wire probes (positive voltage) [8].
5. To prevent crosstalk of secondary electrons in multi-electrode secondary emission monitors [9] (negative voltage).

A very low ripple of the voltage source is required to prevent artefacts in the current measurement [6]. A voltage

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range of ±100 V and a current capacity of 0.3 mA should be sufficient for most applications.

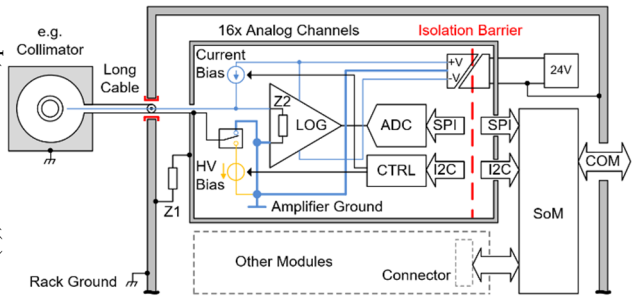

Figure 1: Grounding concept of one isolated log-amplifier channel. By default, the sensor ground connects over a relay contact to the amplifier ground. If a bias voltage is required for a measurement, the HV-supply (yellow) must be turned on and a fixed voltage can be set by a DAC in the range of ±100V. All blue lines are then at the set voltage potential, including the wire into the sensor to measure the current. There is also a bias current option to set a fix current offset for the log-amplifier in the range of 0 to 2.5 nA.

High Voltage Output

At an electrode distance of 7 to 10 mm, a supply voltage of 300 V is sufficient to prevent saturation in the IC at the given loss and radiation levels [1, 6]. The ground of the 300 V sources feeding the IC loss monitors is also provided individually via the long HV cables, in order to prevent coupling of ground loop noise via the electrodes. Each chamber will be supplied by its own HV source. This eliminates the need for low-pass filters at the IC location as used in [6]. Nevertheless, a strong low-pass filter at the voltage source is required to reach a very low ripple.

Signal Processing

Basic signal current sampling of all channels is performed with 1 MSps to keep aliasing filters simple. The signal decimation filters deliver 10 kSps for further processing.

The actual currents are available to the machine control system (MCS) in three instances, low-pass filtered with selectable time constants and binning. In addition, three instances of waveforms with independently selectable number of samples and binning can be measured with different trigger modi and read out en-bloc.

Independently, the signals are evaluated according to several rules defined in firmware, in order to activate an interlock output in case of critical beam conditions. A fast exchange of information between several modules allows using the combined information for more refined rules. Thereby also the information on actually moving wire monitors or beam switching is introduced, to adapt interlock limits to tolerate temporarily modestly increased losses. It also allows comprehensive triggering of waveforms, e.g., in case of interlocks.

Setting of filter and interlock parameters, as well as the read-out of measured data and causes for interlocks will be supported by a separate slower network connection.

Exchange

A temporary coexistence of new and old electronics must be possible, since only a fraction of all modules can be replaced in the annual shut down or at service days.

ELECTRONICS HARDWARE

Hardware Architecture

For the mechanical form-factor, 6U (VME64x), 3U (CompactPCI-Serial) and a custom 19" box were considered. Due to the potential isolation and the build-in DC/DC converters in each current input channel, the circuit requires a relative large PCB. The decision was to use a 19" box that offers a large PCB area, fits into the existing racks, is compact, and cost efficient.

Module Layout

The so-called SoM-LogIV16 module combines at its motherboard 16 current channels with separate grounds, two mezzanine I/O modules, a power supply and a system on module (SoM) on a socket (Fig. 2). One of the mezzanine modules provides 6x TTL inputs, 2x TTL outputs and one specific interlock output. The other mezzanine module provides 8x high voltage outputs. The module is passively cooled.

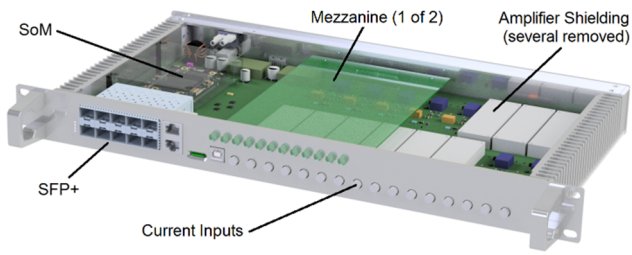

Figure 2: SoM-LogIV16 module layout.

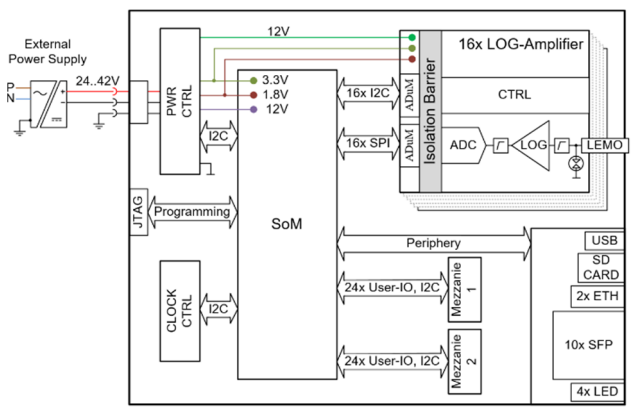

Figure 3: SoM-LogIV16 hardware components.

The motherboard has the following functionality implemented (Fig. 3). A power unit to measure voltage and current of the 12 volt rails, which also protects the electronic against over currents. This is helpful for health management of the system. A flexible clock unit allows configuration of frequencies for hardware and serial protocols. Each current channel is controlled by I2C and SPI interfaces. Galvanic isolation is realized with ADuM252N

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and ADuM1251 from Analog Devices. Beside the controllable 12-bit voltage and current sources, a temperature sensor with 1/16 °C resolution is also present on every channel to compensate temperature dependent current drifts with look-up tables, if needed.

SoM

The SoM-LogIV16 baseboard utilises a sub-set of the available hardware resources on the Enclustra Mercury+ ME-XU1-6EG-1I-D11E SoM [10]. The SoM, built around a Xilinx Zynq UltraScale+ MPSoC device, has three major processing units: Application Processing Unit (APU), Real-Time Processing Unit (RPU) and Programmable Logic (PL).

The APU consists of a quad core Arm Cortex A53 processor (11000 DMIPS). The PRU consists a dual core Arm Cortex R5 processor. The protection algorithms execute on the RPU executing in lock-step mode (830 DMIPS).

Besides being a fully functional hardware computer module, the SoM delivery includes a pre-developed U-Boot boot-loader and an adapted Linux kernel. The physical layers, like Ethernet PHY, are a part of the module and preconfigured in U-Boot. In addition, the Linux device-tree for the module is available from the module manufacturer. This greatly simplifies the development and bring-up of the Linux system.

After Linux has booted on the SoM, the Programmable Logic and the Arm R5 processor are loaded with firmware. The procedure is to load a FPGA binary file and an elf-file respectively. There are drivers available in the Linux system that facilitate the copying of files to predefined locations in the file system.

Even though the Linux system is pre-configured for the SoM, there are extensions to the hardware system on the SoM-LogIV16 baseboard. There are multiplexers, GPIO expanders, DAC's, temperature sensors, programmable oscillators and hot-swap controller - all connected to the I2C controller of the SoM. To get Linux aware of these components, extensions to the device-tree are required. To keep the configuration modular and the Linux system for the SoM reusable for other baseboards, a Linux device-tree overlay defines the extensions on the baseboard. The device-tree overlay is file specific to the SoM-LogIV16 baseboard and is loaded into the kernel after the Linux system has booted. According to the definitions in the devices-tree overlay, drivers for the baseboard components are loaded automatically.

SOFTWARE & FIRMWARE ARCHITECTURE

The RPU is running bare metal in lock-step mode. This configuration gives the RPU large tightly coupled memories suitable to fit the protection algorithms. The code runs out of tightly coupled memory with deterministic access time and high reliability.

The APU has four hardware threads (cores) – each approximately 3x faster than the RPU. The total processing power is 13x that of the RPU measured in Drystone MIPS. The APU is executing Linux SMP with PREEMPT_RT. The APU program is running out of ECC DRAM with memory scrubbing for high reliability. There is limited real-time capability in the default SMP configuration of the operating system due to automatic load balancing. It is therefore important to isolate CPU's executing real-time code. This can be done by utilising a boot parameter (isolcpus=1-3) for the Linux kernel, as well as setting the IRQ affinity manually.

On the PL, an intellectual property (IP) core implemented in VHDL interfaces with 16x 18-bit ADCs (Fig. 4). These are ADS9110 from Texas Instruments, capable of up to 2 MSps. Data is transferred over SPI buses in parallel to be pre-processed on-chip. Data pre-processing in VHDL consists in first time-stamping and then down-sampling data through low-pass filtering or averaging methods.

Then data is forwarded to a common buffer on off-chip DDR4 memory, where it can be accessed from the real-time processors for further post-processing, which are activated with an interrupt.

The IP interfaces directly the DDR memory controller over a 128-bit AXI-Stream interface. This allows more than enough bandwidth to multiplex the 16x ADC channels into the shared buffer.

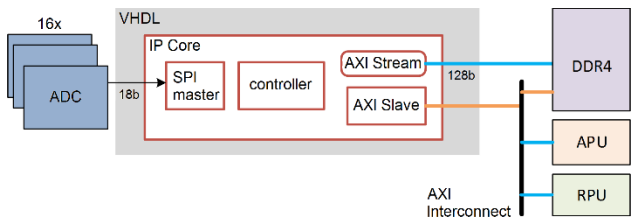

Figure 4: Firmware architecture.

For non-deterministic processing like EPICS one core is used. Three cores are isolated and used for real-time processing. This enables good interrupt latency on the isolated cores and allows rate monotonic tasks up to 10 kHz. All non-critical processing executes on the APU.

Virtual Backplane

The device inter-connection is implemented by means of fibre optical links to provide a fast and secure data exchange between all the SoM-LogIV16 modules. The programmable logic (PL) implements the logic for the Virtual Backplane.

The proposed architecture works logically like a backplane with a shared memory (Fig. 5). When a device writes to the memory, the state of the memory is reflected to all devices in the network. The implementation utilises a distributed memory where a hardware circuit handles the synchronisation.

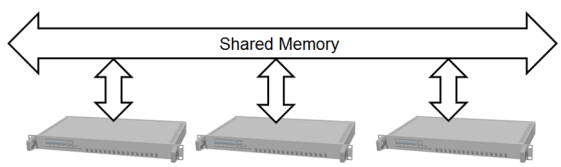

Figure 5: Shared memory.

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Each SoM-LogIV16 includes a network port (Fig. 6) and a number of link ports. The network port and the link ports are connect to a network hub (Fig. 7). The network port is an AXI4 slave component on the internal bus system of the MPSoC [10] device. The link port design al-lows SFP+ fibre optical modules up to 10.3125 Gbps. Even though the hardware supports ten SFP+ modules, we intend to support only three link ports in order to keep the power losses low.

The link encoding is 64B/66B. Each 64-bit block transmits 32 bit of data. This gives 5.0 Gbps of data capacity on the links. There is a block check character (BCC) to detect erroneous packets. Packets with errors are lost. There is no resend or pushback mechanism. All data is sent repetitively at 10 kHz from the AXI4 masters. This makes the network fault tolerant.

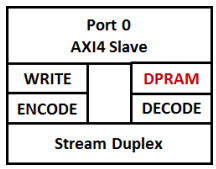

Figure 6: Network Port.

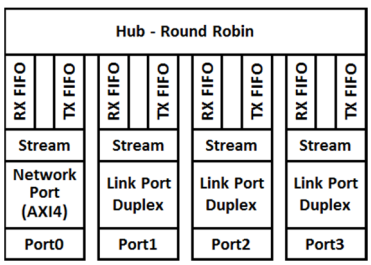

Figure 7: Network Hub.

FIRST MEASUREMENTS

First tests were performed with two evaluation boards with an Analog Devices ADL5304 logarithmic amplifier [11] with a 10 pA to 10 mA dynamic range (Fig. 8).

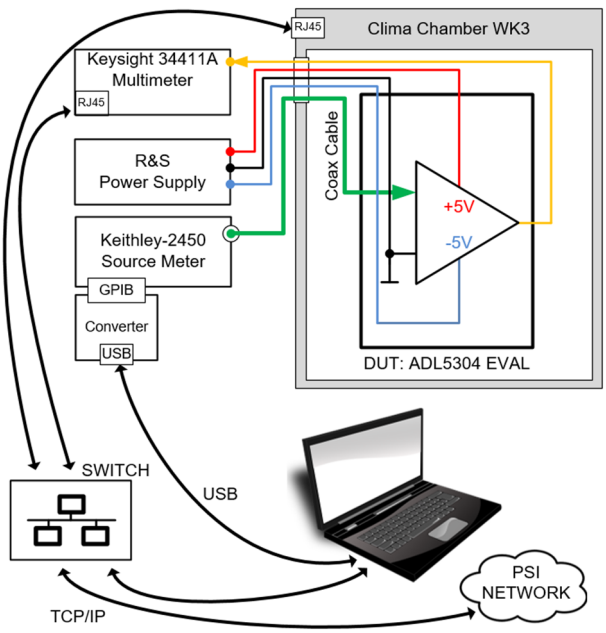

Figure 8: Test setup.

Both samples showed similar results. We find the ADL5304 to be more sensitive to temperature changes (Fig. 9) than to humidity, but the dependency is still very small. This will be corrected, as in the VME based modules [5], with individual look-up tables. Other parameters, such as the current dependent bandwidth, and the response to small positive currents following a negative current input, still have to be determined. A test with both sample inputs coupled in parallel showed that the current range can be extended to 20 mA. The current sum is correct although the current distributes unequally at lower currents.

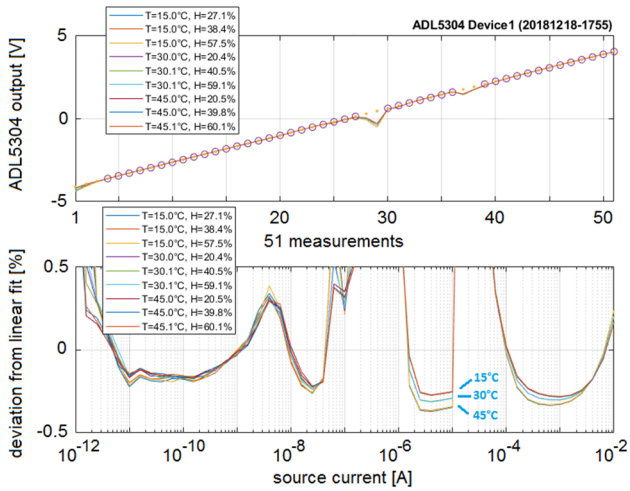

Figure 9: Linearity at different temperatures. The larger deviations do not stem from the logarithmic amplifier, as a test with a different source meter (with different deviations) confirmed. The reason still has to be determined. Despite this, the accuracy over the whole sweep range is in the range of ±0.5%.

OUTLOOK

We intend to produce and test a zero series in the machine in 2020, and to produce a series of 50 pieces and start commissioning in 2021.

AUTHOR CONTRIBUTIONS

RD provided requirements and specifications from diagnostics and operation and wrote the paper with contributions of the other authors. EJ organized the project, guided the development and provided the general architecture. MR developed and tested the electronics hardware, WK and DL contributed concepts and firmware implementation. All authors verified the paper.

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