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CHARGE DETECTION SYSTEM FOR THE CLARA/VELA FACILITY

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Abstract

The CLARA/VELA facility at Daresbury Laboratory combines an FEL test facility and an electron accelerator for scientific and industrial applications, capable of providing up to 40 MeV electrons, with an eventual goal of 250 MeV. Accurate measurement of the bunch charges in a wide range (1 - 250 pC) at a repetition rate up to 400 Hz is required. We present a new system of analogue electronics developed to interface with existing and future bunch charge measurement devices (wall current monitors, Faraday cups, etc.) to measure the bunch charges accurately and precisely. The system is based on a charge amplifier with switchable sensitivity, dark current gating and on-board self-calibration. Results of circuit simulations, offline calibration tests and online beam tests of a prototype system are presented.

INTRODUCTION

The CLARA front-end is the first phase of the CLARA 250 MeV FEL test facility, based at Daresbury Laboratory. The front-end was commissioned during 2018 [1] and used to provide high energy electrons for experiments using the VELA beamline during 2018 and 2019 [2]. The combined CLARA/VELA facility currently incorporates two Wall Current Monitors (WCMs), four Faraday Cups (FCs) and one Integrated Current Transformer (ICT) for bunch charge diagnostics, and plans for the full CLARA facility include several additional FCs and ICTs. The existing charge diagnostics system installed on the CLARA/VELA FCs and WCMs is based on an *LC* integrator circuit with a resonance frequency of 30 MHz [3]. The implementation of this system used on VELA, and the CLARA front-end, lacks important features; such as online and automatic calibration, and remotely controlled sensitivity. This paper presents progress on an upgraded system for signal conditioning and charge detection for these systems, to improve the reliability and accuracy of bunch charge measurements available for commissioning and experimental exploitation of the CLARA beam.

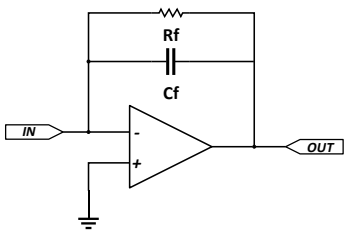
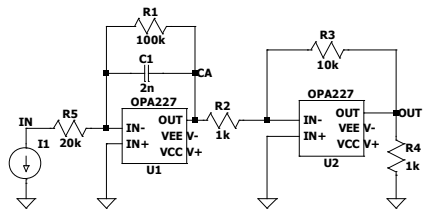
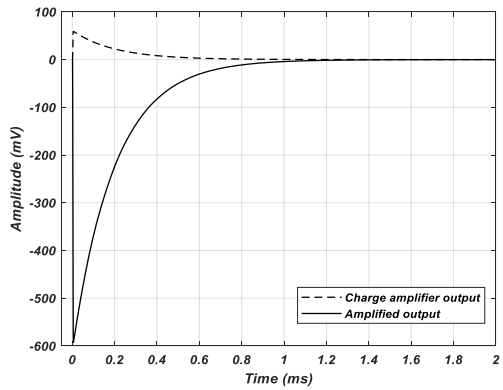


Figure 1: Practical charge amplifier circuit.



(a) LTspice model of a charge amplification circuit



(b) Pulse response of the above circuit

Figure 2: Simulation model of a charge amplification block, and the circuit response for a 120 pC pulse.

The upgraded charge detection system is based on a charge amplifier, effectively a current integrator, in which the voltage amplitude of the output is proportional to the injected charge. Additional features planned for the upgraded system include a current detection mode, dark current gating to avoid saturating the charge amplifier and differential signalling from the accelerator tunnel to protect against picked-up noise.

CHARGE AMPLIFER

A basic, practical charge amplifier briefly consists of an operational amplifier, with an *RC* feedback network, as shown in Fig. 1. The sensitivity, v_o/Q_i, is inversely proportional to the feedback capacitance, C_f. The feedback resistance, R_f, prevents drift due to noise. The combination of capacitance and resistance values determines the fall time of the output signal.

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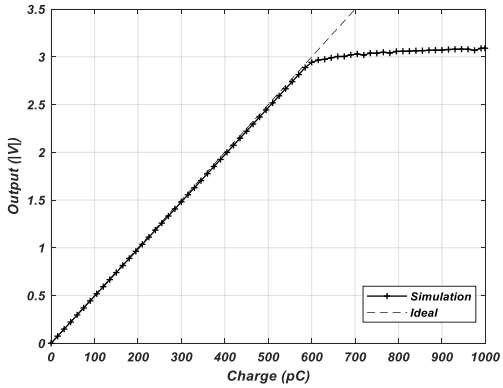

Figure 3: Simulated output amplitude as a function of charge. Note that the absolute value of the amplitude is used for clarity.

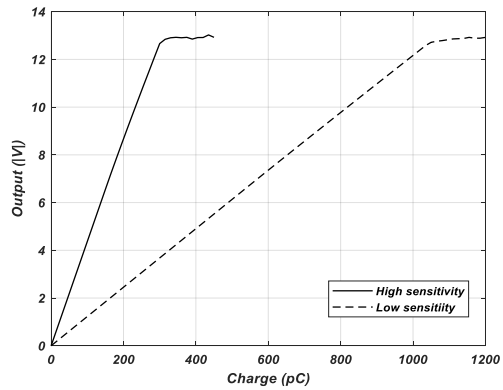

Figure 4: Simulated response of the prototype circuit.

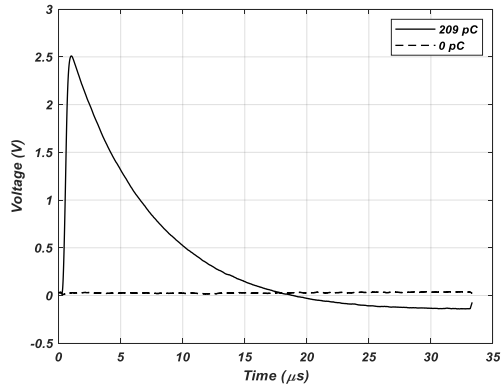

Figure 5: Digitised waveforms from bench-top prototype.

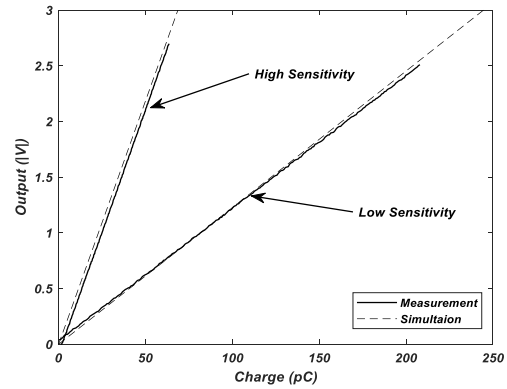

Figure 6: Calibration sweeps for both high and low sensitivity, compared to simulated response.

To maximise the signal amplitude during transmission from the accelerator tunnel to the digitisation equipment, a second inverting amplifier with a gain of 10 was added after the integration stage. A SPICE-based circuit simulator (LTspice) [4] was used to simulate the charge amplification circuit shown in the Fig. 2a, to verify the circuit's agreement with the theoretical calculations. Figure 2b shows the pulse response of the circuit for a 120 pC pulse.

The circuit in Figure 2a has an overall sensitivity of 5 mV/pC and is expected to saturate when the output reaches 3 V, which corresponds to an input of 600 pC. Figure 3 shows the simulated response of the circuit as a function of charge, up to 1000 pC, compared to the ideal response, with saturation close to the expected value.

PROTOTYPE

Based on the initial results, a prototype was built and tested, both offline and later using one of the CLARA/VELA facility's FCs. The prototype was designed with two sensitivity settings, on-board calibration circuitry and dark current gating. Digitisation was via a Red Pitaya's 14 bit, 125 MHz ADC, which was synchronised to the machine timing system, and control achieved using its digital I/O ports. This prototype was powered by ±15 V rails, and included an amplifier stage with a gain of 25. The feedback capacitances were 2 nF and 540 pF for the low and high sensitivity modes respectively. The expected sensitivities were 12.5 mV/pC, with saturation at 1,040 pC for the low sensitivity mode, and 46.3 mV/pC, with saturation at 280 pC for the high sensitivity mode. Figure 4 shows the simulated responses of both ranges to a charge sweep.

The calibration circuit is based on charging a capacitor, of a known capacitance, C_{cal}, to a known voltage, V_{cal}, and then discharging the stored charge, $Q_{\mathrm{cal}} = V_{\mathrm{cal}} C_{\mathrm{cal}}$, into the circuit. A digital 8-bit potentiometer is used to control the voltage and a separate voltage reference is used for each sensitivity setting. The calibration range for the prototype circuit was from 0 pC to 209 pC and 63.75 pC, for low and high sensitivity respectively. Figure 5 shows the output

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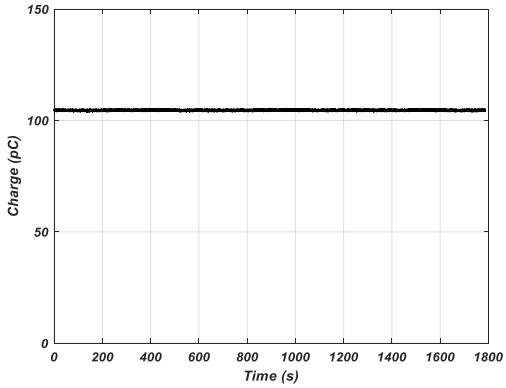
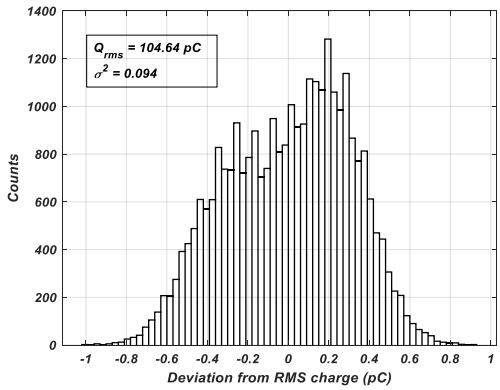


(a) Measured charge over 30 minutes



(b) Histogram of deviation from RMS charge over 30 minutes

Figure 7: Benchtop stability test of prototype circuit.

waveforms of the prototype at maximum and zero calibration charge, for the low sensitivity mode. Figure 6 shows the output voltage for both calibration sweeps, compared to the simulated values. Figures 7a and 7b show measurements where the charge was kept constant for 30 minutes on a lab bench, demonstrating that the charge measurement is repeatable to within 1 %.

The same prototype was installed at the SP1 FC on CLARA/VELA, indicated on the schematic in Fig. 8, with the existing charge diagnostic system, already installed at the WCM, used as a cross-calibration source. A half-wave plate attenuator in the photoinjector laser transport line was used to vary the bunch charge, Fig. 9 shows the measured charge at both the WCM and FC over 1900 shots, or just over three minutes. In Fig. 10 the RMS charge detected at the nine different half-wave plate settings is shown. Figure 11 shows the waveforms from the prototype, when it is installed on the CLARA/VELA accelerator. The difference between the measured charge at the WCM and FC ranges from 3.16 pC, at low charge, to 1.15 pC, at high charge, with a mean difference of 1.65 pC. There is no single, definite reason for

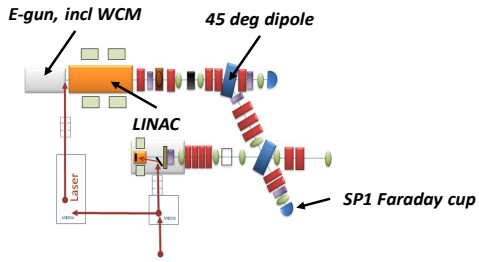


Figure 8: Schematic of CLARA/VELA, with the WCM and FC used for cross-calibration indicated.

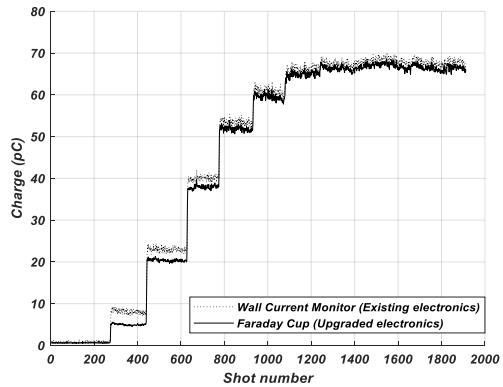


Figure 9: Measured charge over 1900 shots on CLARA/VELA.

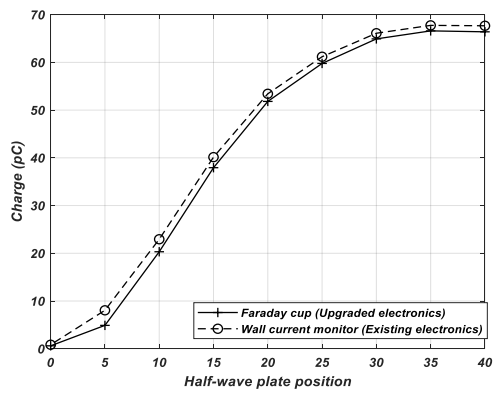


Figure 10: RMS charge at different half-wave plate positions.

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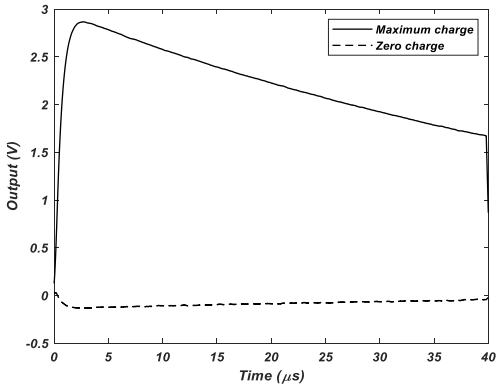

Figure 11: Measured waveforms from the prototype charge amplifier when installed on CLARA/VELA.

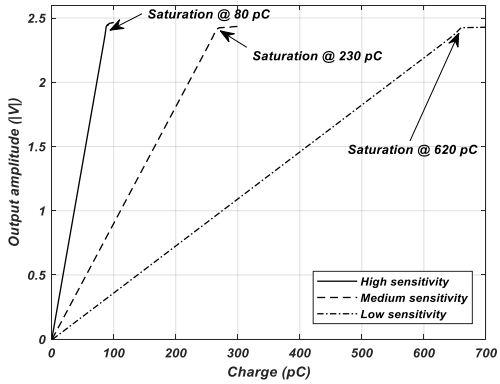

Figure 13: Simulated response to charge sweeps for the final design.

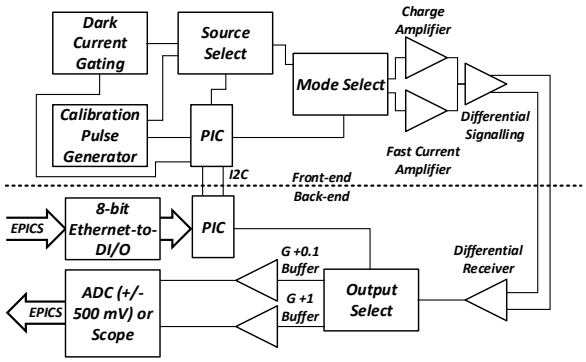

Figure 12: Bandwidth of fast current detection mode.

this difference, but the main hypothesis is a combination of imperfect charge transport and the digitisation not capturing the "true zero" due to the positive charge injection by the gating switch shown by the dip in the voltage at zero charge in Fig. 11.

FUTURE PLANS

The plan is to install and commission a system based on the charge amplifier described above in preparation for the 2020 block of experimental exploitation of the CLARA/VELA facility. This system is planned to have additional features compared to the prototype system above, and will be closely integrated with the timing system and machine control system. Additional features to be included in the complete system include: (a) Three sensitivity ranges (5 mV pC^{-1}, 12.5 mV pC^{-1} and 50 mV pC^{-1}, corresponding to saturation at 620 pC, 230 pC and 80 pC respectively), (b) a fast current detection mode, (c) pulse and sweep calibration modes from zero charge to saturation, (d) differential signalling from accelerator tunnel to processing room, and (e) selectable attenuation (G = +0.1) to comply with ADC input range requirement. Figure 12 shows a block diagram of the planned system, while Fig. 13 shows the peak output amplitude as a function of charge for each of the ranges, from an LTspice simulation of the full system.

CONCLUSION

A design of an upgraded charge diagnostics system for the CLARA/VELA facility is presented. Using LTspice simulations, the proposed pre-amplifier was shown to closely agree with ideal calculations. Bench-tests of a constructed prototype further demonstrated its close agreement with simulation and theoretical calculations. The prototype system was also tested successfully on CLARA/VELA, by cross-referencing with the existing, calibrated wall current monitor. An overview of the complete system is presented alongside simulations of its operation, and plans for its installation and commissioning before the next period of experimental exploitation in 2020.

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