THE SPS Wideband Feedback Processor

A Flexible FPGA-Based Digital Signal Processing Demonstration Platform for Intra-Bunch Beam Stability Studies

IBIC 17

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Talk Outline

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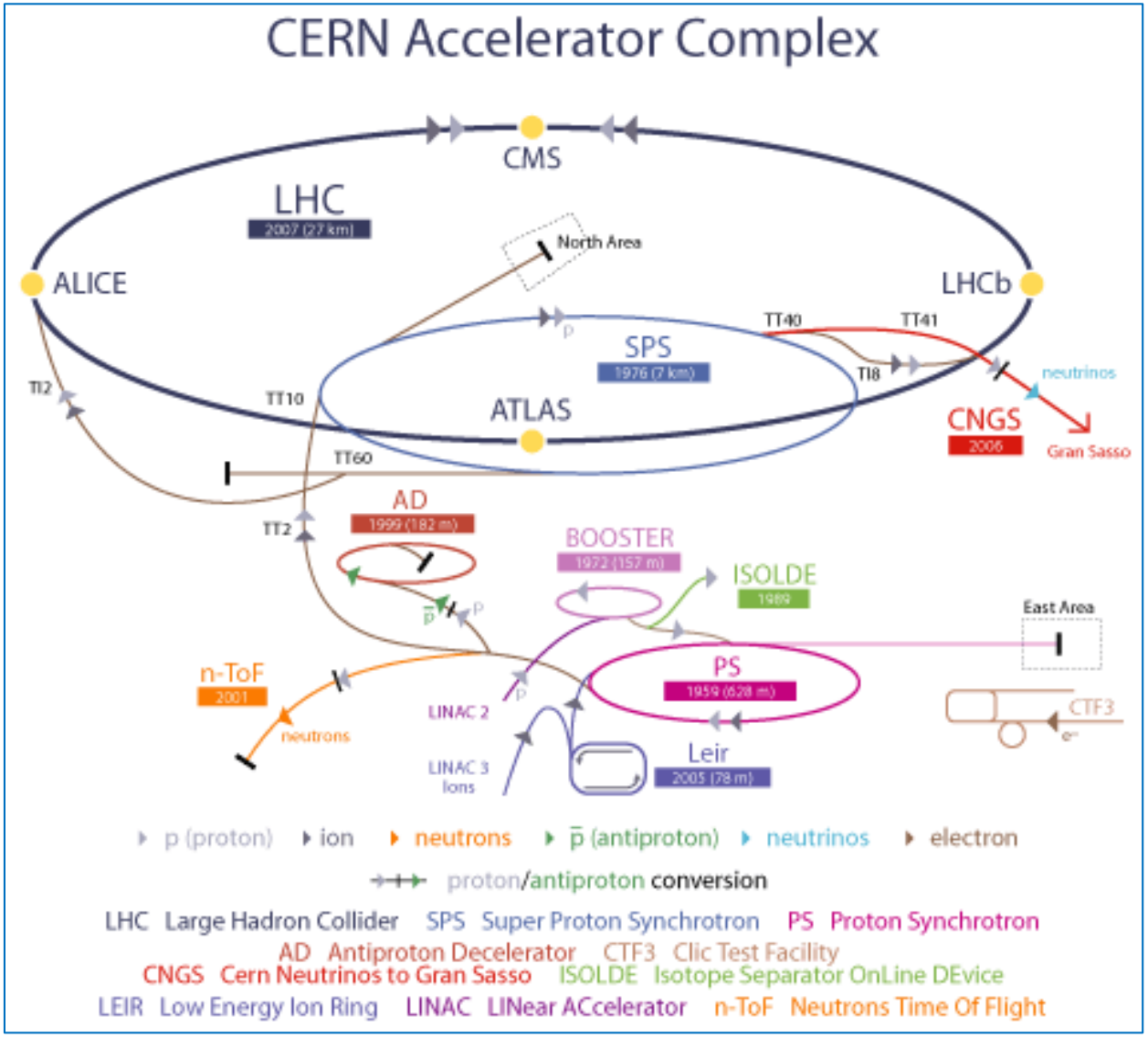
1) Introduction
2) System Overview
3) The Feedback Processor
4) Operational Examples
5) Upgrades & Next Generation

The SPS



The CERN Super-Proton Synchrotron:

- Last machine in the LHC injection chain / Normal-conducting
- 6.9km circumference
- Takes Protons from PS at 26 GeV and accelerates them up to 450 GeV for extraction to the LHC
- Beam bunch length:
  - ~4ns @ injection
  - ~2ns @ extraction
- Bucket Width: 5ns
- Bunch Spacing: 25ns (5 buckets)
- LHC Beam: Served up in 4 batches, with each batch consisting of 72 bunches/batch (batches separated by 45 buckets) 288 Bunches Total

This project is a collaboration between CERN & SLAC

Source of images: CERN

Motivation for this Work

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→ *Why* are we doing this *how* we do it and *what* makes it Challenging?

- The LHC Injector chain is undergoing an upgrade for increased intensity (more luminosity) / LHC Injectors Upgrade (LIU) project for the High Luminosity LHC (HL-LHC) Program

- At these higher beam intensities, studies suggest that transverse *intra-bunch* instabilities in the SPS will limit Lumi

- SPS Transverse instability control – 3 Methods:
  - Machine lattice modifications,
  - Vacuum chamber coating (amorphous carbon),
  - Active feedback control
    - **Intra-Bunch** Stabilization feedback control -- measure, process, and control motion *within* the 2ns proton bunch

- How:
  - We measure the motion *within* the bunch by sampling very fast: 4GSa/s (250ps sample spacing), producing 16 samples (or slices) across 5ns beam bucket width, then compute corrections and apply back onto the beam

Engineering Challenges

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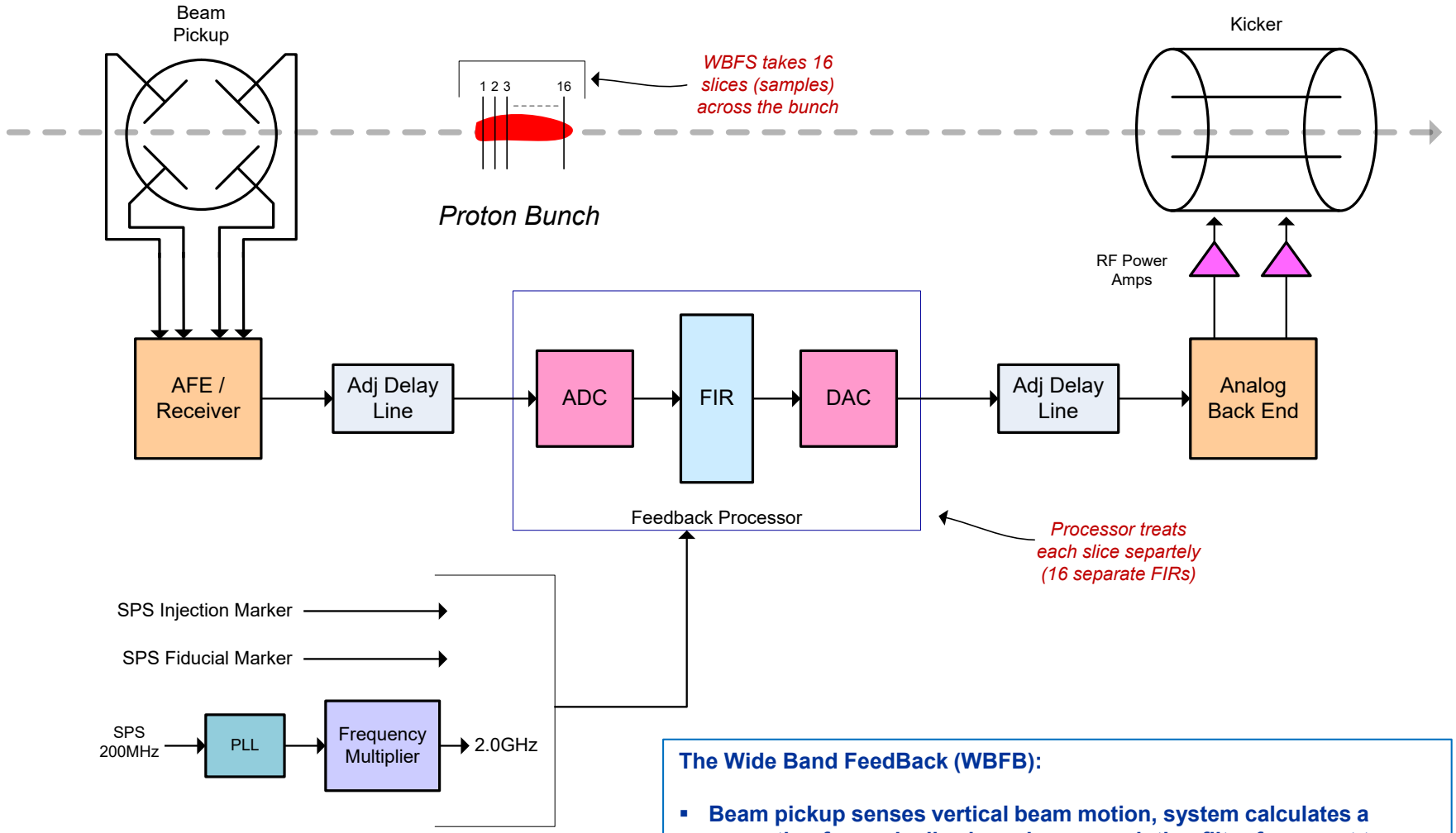
→ **Engineering Challenges**: High Bandwidth (1GHz) System Required

- Wideband Pickups, Kickers, Power Amplifiers
- Wideband RF processing electronics (Front- and Back- ends)
- Wideband, High Sampling Rate (4GSa/s) Data converters
- High-Speed digital electronics for signal processing

- Note: The 1GHz WBFB is for Intra-bunch instability control.
  - This complements the existing SPS transverse damper (lower BW -- 20MHz), which controls coupled bunch instabilities

System Overview – Transverse Feedback

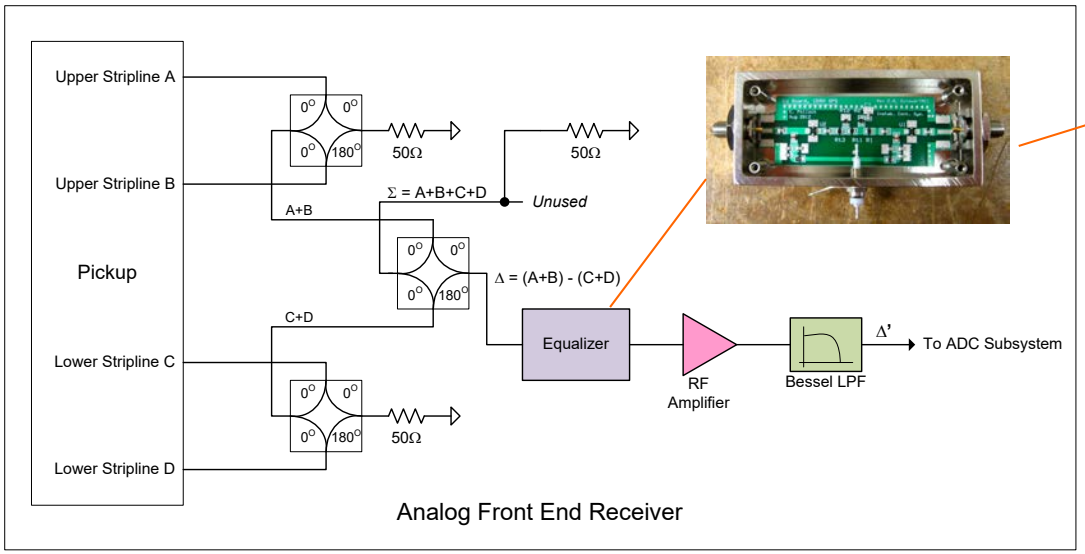


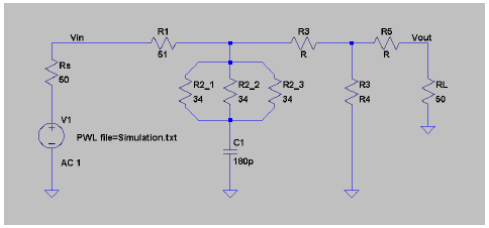
Prototype Demonstrator System

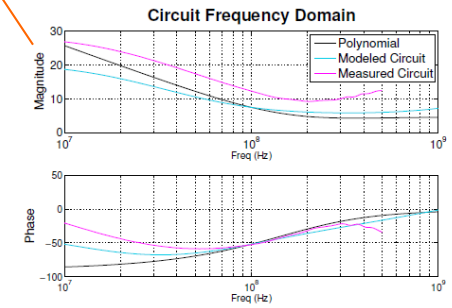
The Wide Band FeedBack (WBFB):

- **Beam pickup senses vertical beam motion, system calculates a correction for each slice based on convolution filter from past turns**
- **System measures and corrects the *Intra-bunch* motion, taking 16 slices (samples) across the bunch in a 5ns sampling window (4GHz sampling / 250ps spacing) as opposed to treating the bunch as a single oscillating entity**

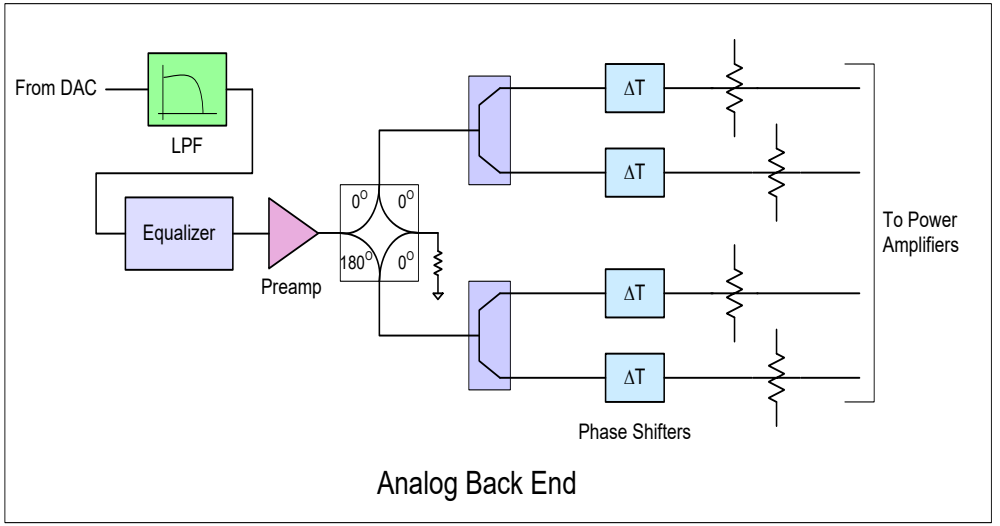
System: AFE / ABE





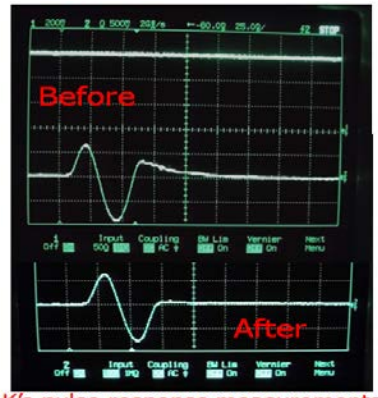


- **Analog Front End:**
  - **Hybrids combine exponentially tapered stripline pickups, create Δ & Σ outputs, Δ used for vertical displacement measurement**
  - **Equalizer corrects for phase distortion on Pickup & Cable plant**
- **Analog Back End:**
  - **Equalizer performs similar fcn as in AFE**
  - **Preamps drives signal to power amps in tunnel**

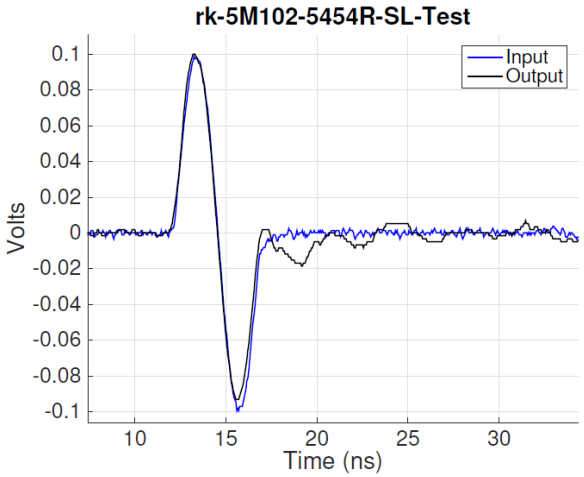


System: RF Power Amplifiers

- The Kicker is driven by RF Power Amplifiers (Pwr = 1KW, BW = 20MHz…1000MHz)
- Our Application (pulsed mode) requires that the RF Power Amplifier has good transient time-domain performance. This characteristic is typically not specified or tested for by manufacturers who are concerned with modulated CW operation.
- Several different units were evaluated, with R&K Company Limited (Fuji-City, Japan) demonstrating the best performance
- Biggest concern with amp is radiation effects in SPS tunnel / We have fully characterized the new R&K amps to get a baseline on their performance prior to installation at CERN



R&K's pulse response measurements

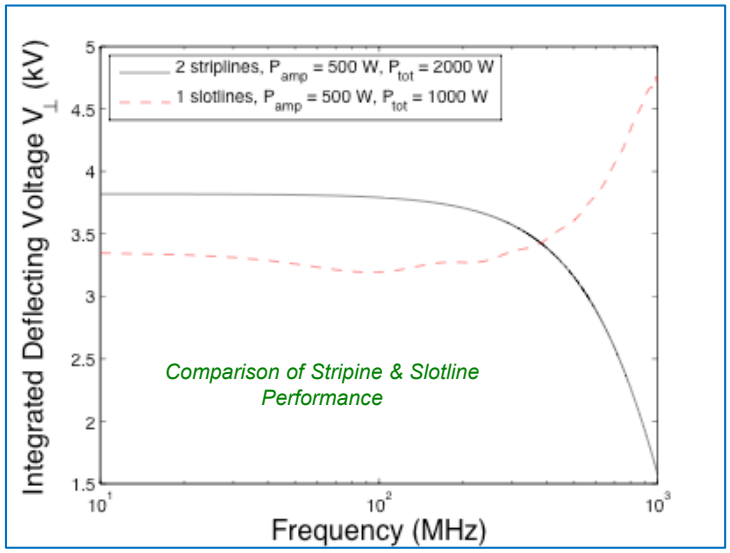


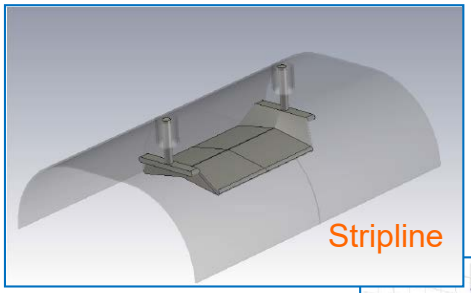
System: Beam Kicker

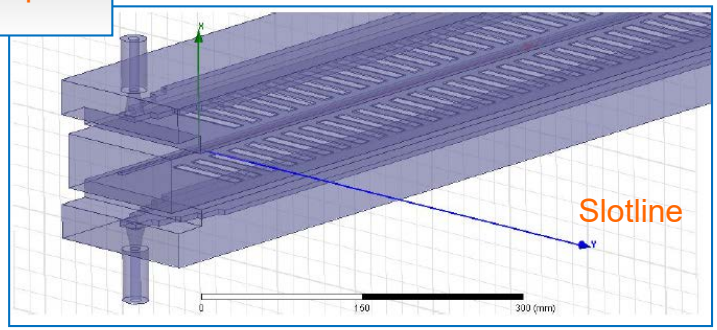
- The current stripline kicker at the SPS has 500MHz BW. limits control to lower-order modes (0, 1, 2)

- A design effort for a 1GHz, 1KW kicker was conducted, culminating in a design report (J. Cesaratto, SLAC Toohig fellow). Studied three different kicker designs: Cavity, Stripline and Slotline.
  - The report suggested pursuing the Stripline (better performance at low frequency) and Slotline (slightly lower kick strength, but response is full 1GHz BW) designs.

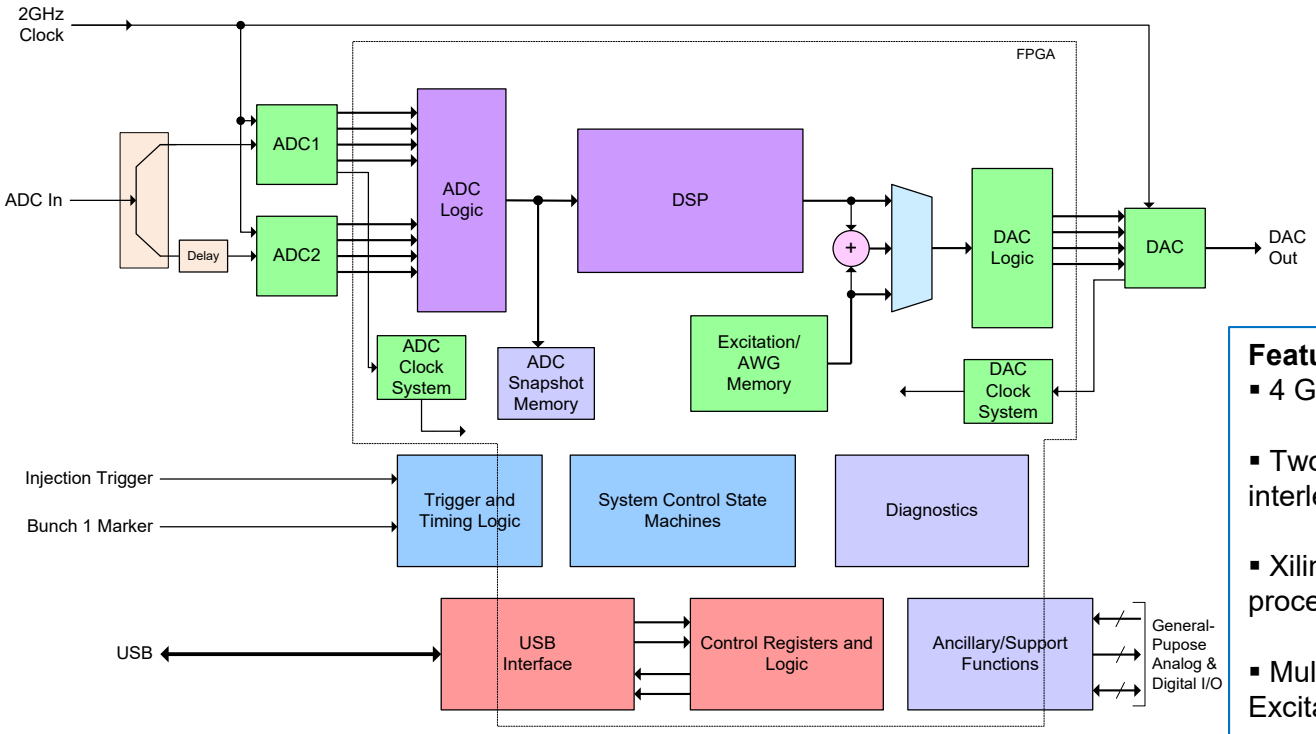
- The Slotline Design is being fabricated at CERN for installation in 2018







The Feedback Processor



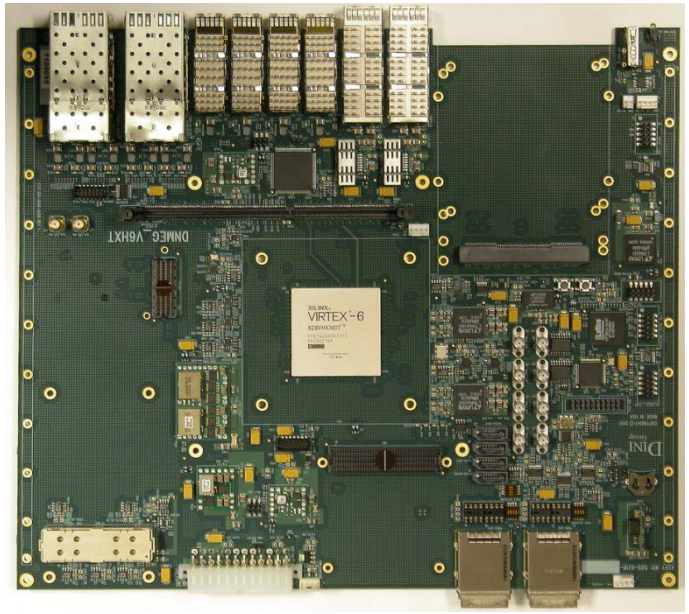
Feedback Processor Demonstrator Block Diagram

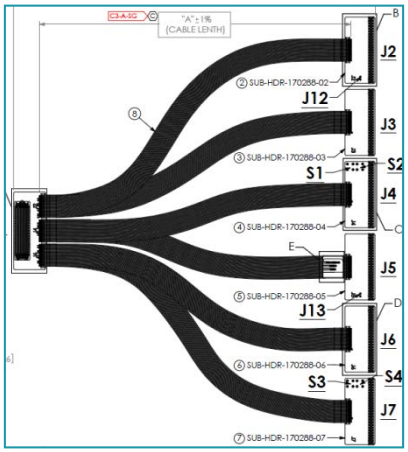
Features: **Expandable/Flexible Platform**

- 4 GSa/s DAC
- Two Maxim 2GSa/s (2.2GHZ BW) ADCs interleaved to get 4 GSa/s
- Xilinx Virtex-6 FPGA for all digital signal processing, acquisition, diagnostics & control
- Multi-mode operation: Feedback channel -or- Excitation/AWG
- Timing and Trigger processing
- Diagnostics include:
  - ADC Snapshot memory
  - Trigger rate and missing trigger
  - DSP Saturation Indicator
- USB 2.0 Interface to host
- Packaged in a 7U, 19-inch rack mount chassis

Feedback Processor – Hardware

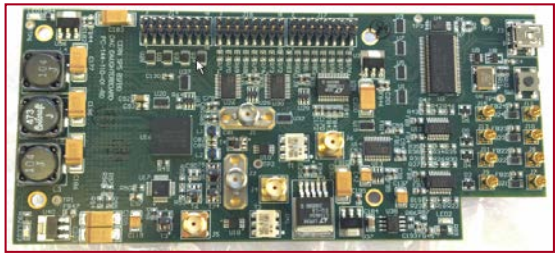
Commercial FPGA Motherboard

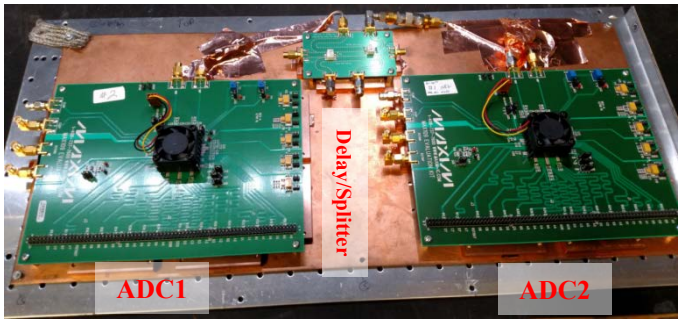




Custom High-Speed ADC Interface Cable Assembly (made by Samtec, Inc.)

Custom DAC Daughterboard

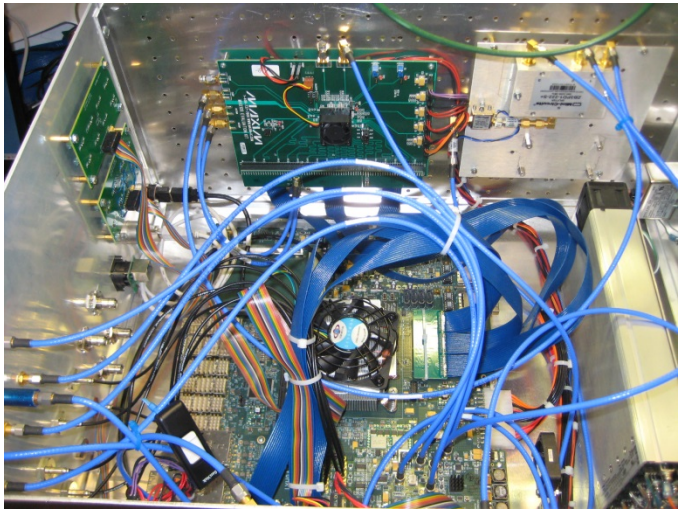




Maxim ADC Eval Boards Mounted to Grounding place

Hardware:

- **Mixture of Custom and Commercial HW:**
- *Enabled a working system to be assembled quickly*
- Modular Design (ADC / DAC / FPGA Engine)
- Commercial FPGA Motherboard using Xilinx Virtex-6 (XC6VHX565T – largest device in family 567000 logic cells, 864 DSP Slices)
- Custom DAC Daughterboard (designed at SLAC)
  - Uses Maxim MAX19693 12-bit 4 GSa/s DAC
  - Also contains USB Interface, Clock, Trigger & Strobe Circuitry
- ADC:
  - Uses Two Maxim MAX109 2GSa/s (2.2GHz BW) 8-bit ADC Eval Boards interleaved to get 4 GSa/s
  - Custom ADC interface cable developed with and built by Samtec Inc.

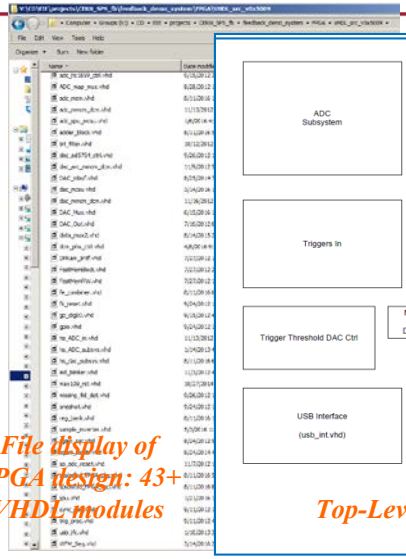


FB Processor Demo Unit Chassis internal view

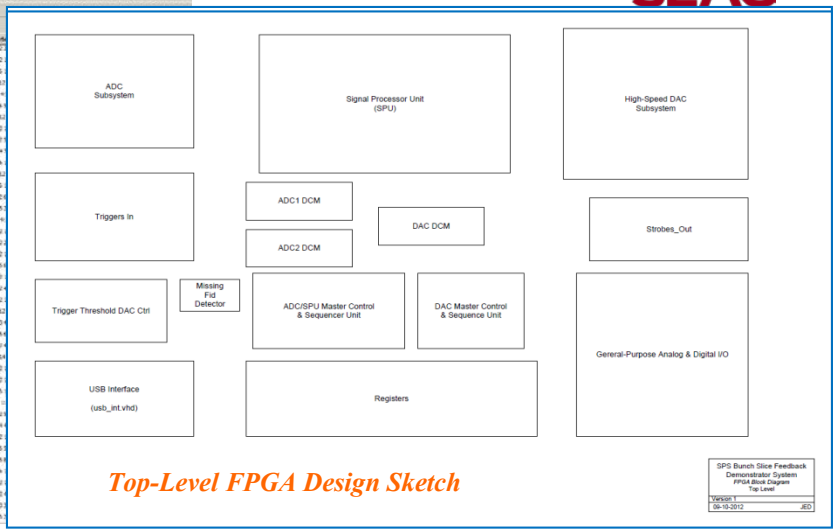
Feedback Processor – FPGA Gateware

FPGA Gateware (Firmware):

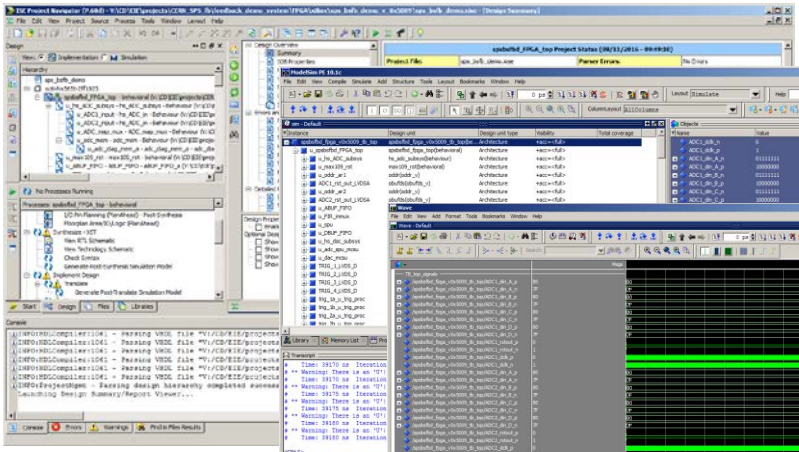
- **This is the LARGEST development effort**:
  - 46 VHDL modules written plus IP blocks from vendor
- Design developed in straight VHDL (text entry) / Synth & Compile with Xilinx ISE
- Some device-specific IP blocks (memory, FIR filter)
- Design is modular so one can “plug-in” new blocks / features
- DSP Block: (16) 16-Tap FIR Filters (treat each slice as a separate oscillator)
- Current design uses up 50% of on-chip DSP blocks
- Can process 64 Bunches (limited by Xilinx IP block) of 288 bunch SPS LHC fill
- Design compiles to 300MHz so we can easily run at 4GSa/s



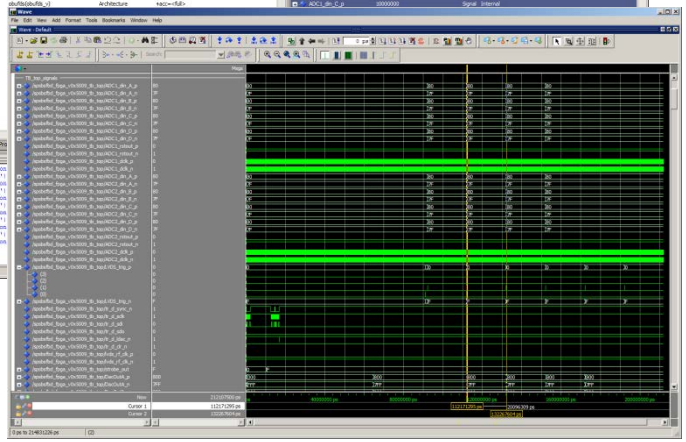
File display of FPGA design: 43+ VHDL modules



Top-Level FPGA Design Sketch

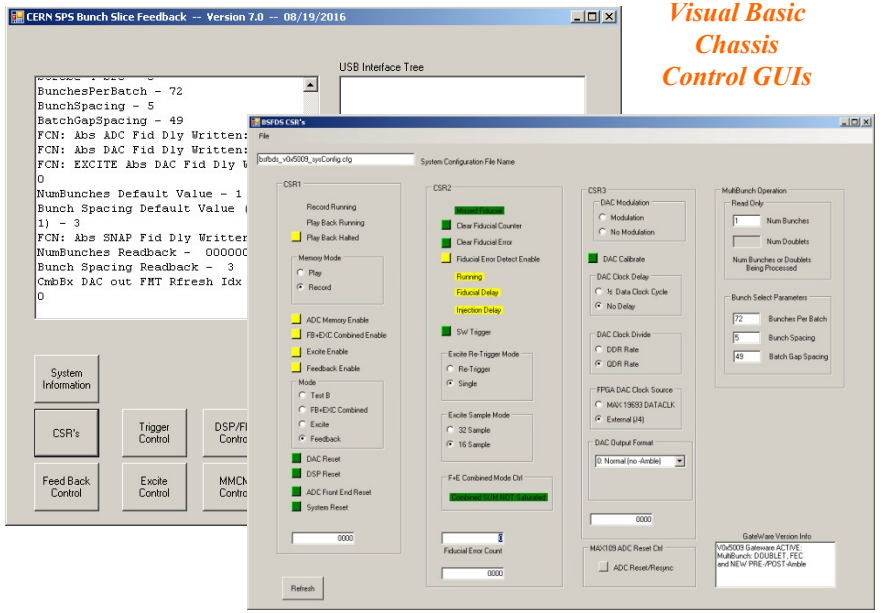


Xilinx ISE FPGA Builder Tool

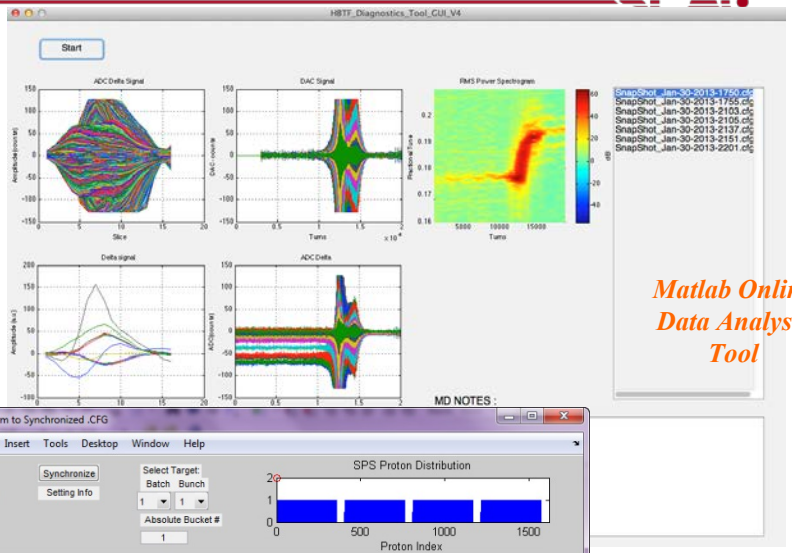


ModelSim FPGA Simulation Tool

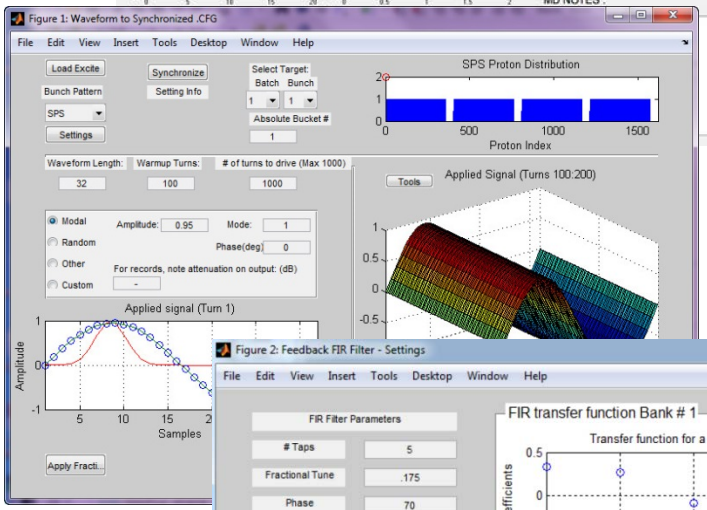
Feedback Processor – Software



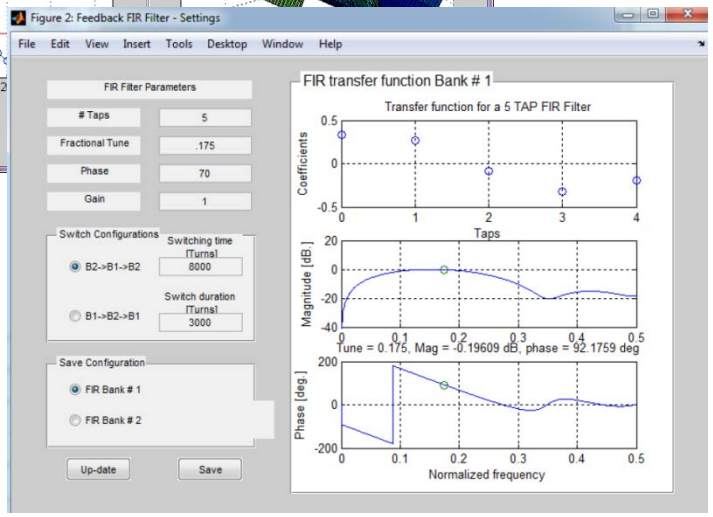
Visual Basic Chassis Control GUIs



Matlab Online Data Analysis Tool



Matlab Excitation Waveform Designer



Matlab Feedback FIR Filter Designer

System Software (two sets):

This user-friendly suite of applications is what we use when operating the system:

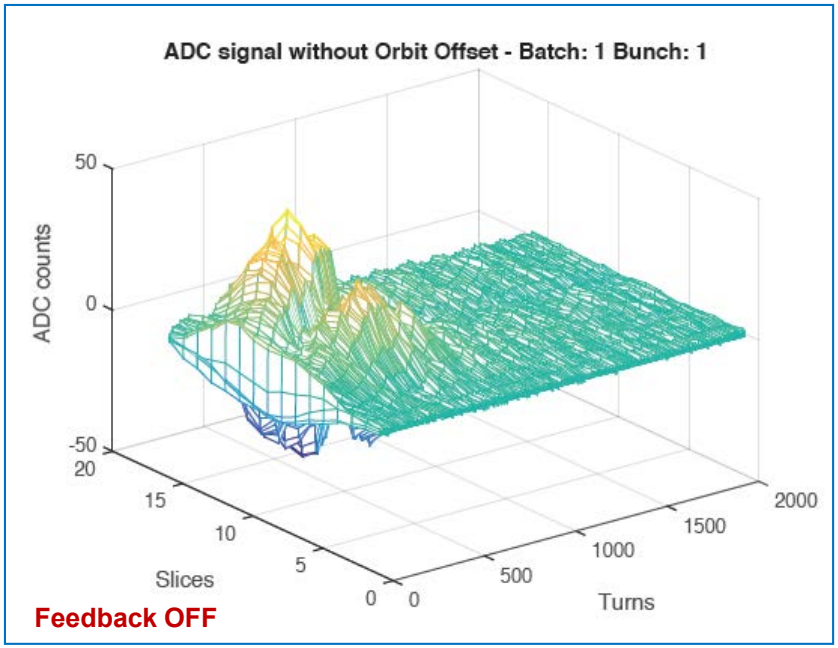
System User Interface and Control (Visual Basic):

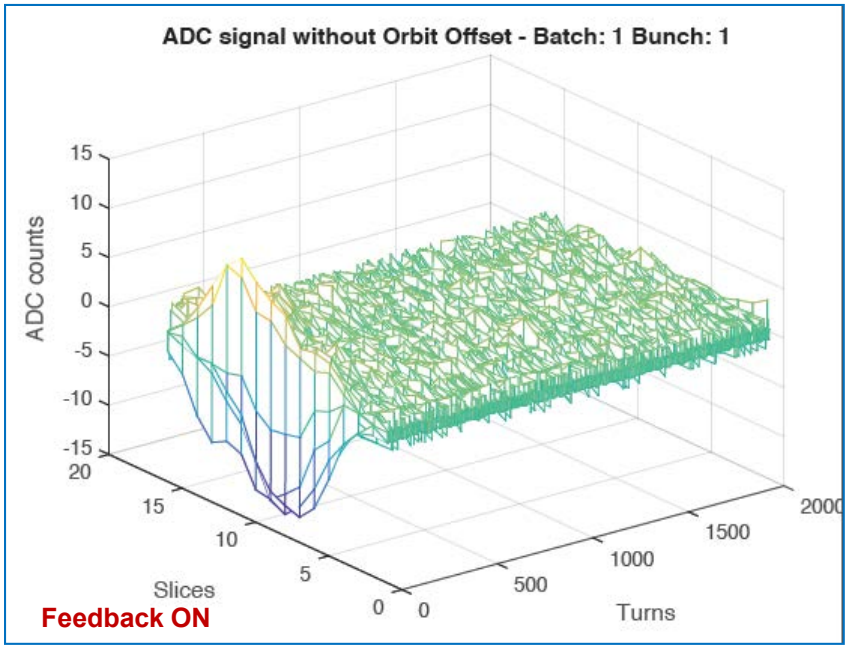
- Developed with Microsoft Visual Basic.NET (2010 version)
- Interfaces to custom Matlab tools via configuration files
- SW is smart and recognizes & responds to different GW versions

Design and Analysis Tools (Matlab):

- Many tools have been created (offline & online)
- Excitation Waveform Designer
- FIR Filter Designer
- On-Line Data Analyzer (looks at Snapshot data)
- Plus many, many offline analysis tools

Operational Example 1

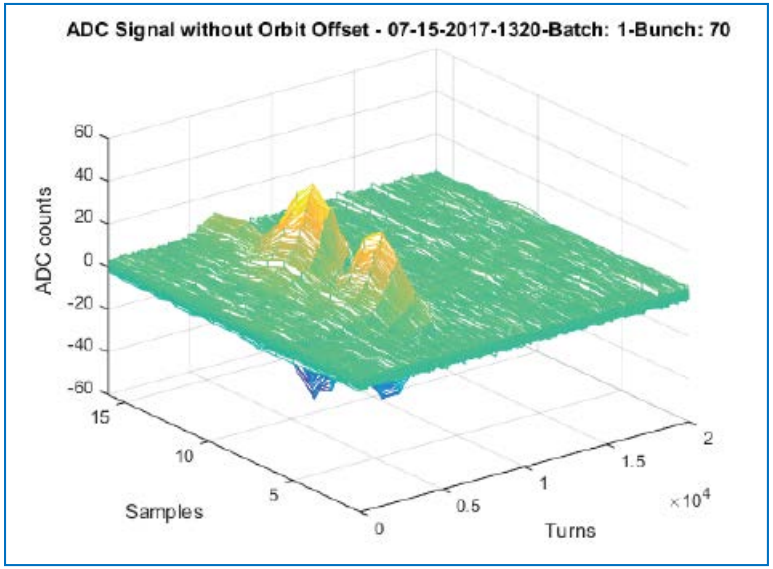


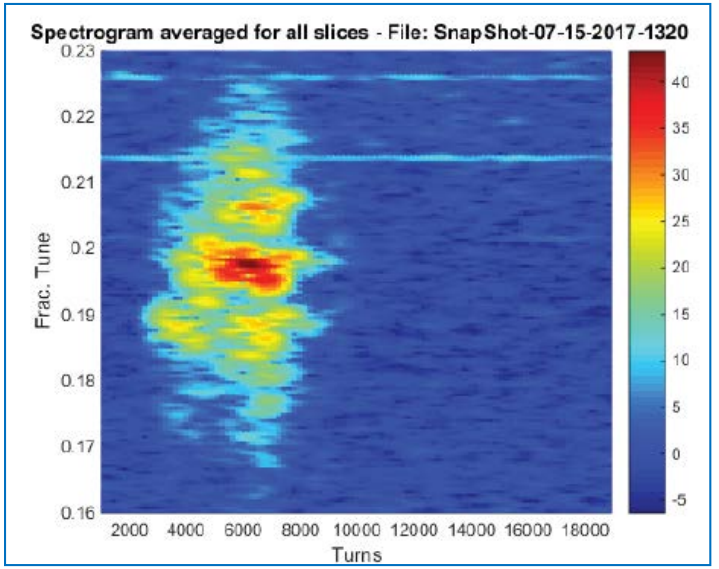


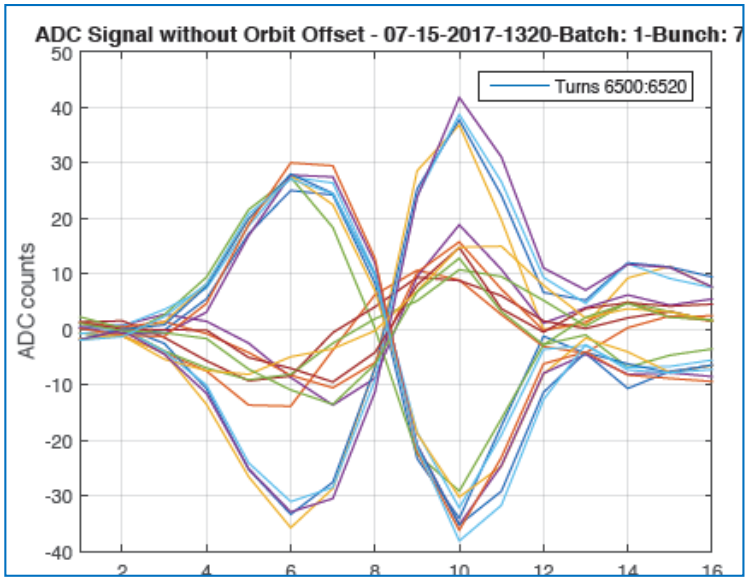
2016 SPS MD -- Example of Mode 1 Oscillation Damping

- **SPS Setup: single-bunch beam**
- **Beam Intensity: 2.0E+11 PPB, Q26 lattice (low chromaticity)**
- **Left-Hand Plot: FB OFF / Injection transient damps, but mode 1 (head-tail) intra-bunch oscillation grows rapidly, charge loss between 400…800 turns**
- **Right-Hand Plot: FB ON / Injection transient quickly damped down in < 200 turns, No intra-bunch oscillation develops, No charge loss**
- **Data recorded using WBFS snapshot diagnostic, captures all slices on all turns, DC orbit offset removed post record, data is plotted turn-by-turn**

Operational Example 2







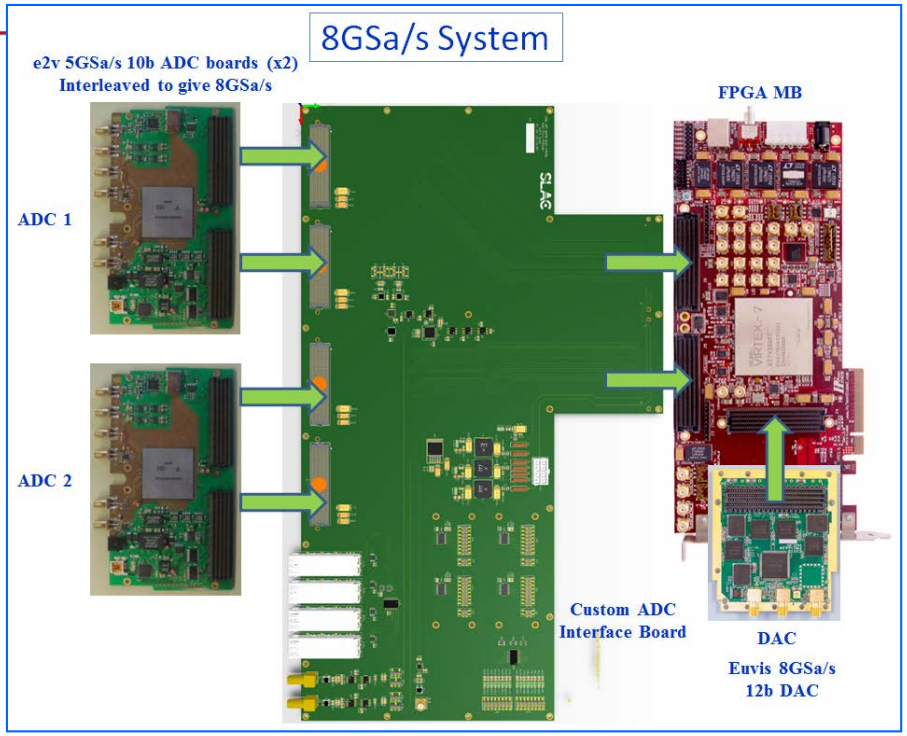
2016 SPS MD – Driven Mode Study

- **SPS Setup: Multi-Bunch (observing bunch 70)**
- **Bunch is excited by shifting to positive feedback on turns 3000…6500, 6500 & onward is damping (complete damping in ~1000 turns) / -FB → +FB → -FB**
- **Surface plot shows Mode 1, some Mode 2**
- **Spectrogram shows mode 1, some mode 2, hints of mode 3**
- **Lower Left: Equalized pickup signal shows head-tail structure within the bunch (seeing all 16 slices) over 20 turns**

System Upgrades & Next Generation

WBFB Upgrades – Existing 4GSa/s System

- **Active DC Orbit Offset removal mechanism**
- **Use Motherboard DDR3 memory for mult-bunch & many-turn snapshot recording**
- **Ethernet interface for faster data transfers, remote operation**



Next Generation WBFB – 8GSa/s

- **Technology has advanced (ADC/DAC/FPGA) to where now am 8GSa/s system is viable**
- **8GSa/s :**
  - Higher BW allows control of more modes (anticipating higher BW backend)
  - More samples per bunch provides more detailed diagnostic information
  - Processing of shorter bunches (e.g. LHC)
  - Enabled different feedback configurations: (e.g. two pickups)

The 8GSa/s effort was funded by the US-Japan Cooperation Program in High Energy Physics

- **Prototype system is in development (commercial ADC/DAC/FPGA boards) / Custom ADC Interface board developed**
- **ADC: Two interleaved 10b, 5GSa/s (3.2GHz BW) Devices**
- **Custom ADC Interface board developed, awaiting funding for fabrication**
- **FPGA development, system packaging also awaiting funding**

End of Talk

Thank you for your attention!

Project Contributors

SLAC

SLAC:

John Fox	PI, Project Lead
Claudio Rivetta	FB Control, Sim & Modelling, Measurements
John Cesaratto	Toohig Fellow, Sim & Modelling, Kicker Design, Meas
Ozhan Turgut	Stanford Astro/Aero Grad Student – Optimal Control (thesis topic) / Sim & Modeling
John Dusatko	System HW/GW/SW Design
Jeff Olsen	System SW

CERN:

Wolfgang Hofle	BE-RF-FB Group Lead, Lead collaborator
Urs Wherle	System Integration and support
Gerd Kotzian	Transverse Damper, pickup studies
Endre Bjorsvik	Transverse BQM, SPS system integration
Elias Metral	Accelerator Physics
Kevin Li	Accelerator Physics
Hannes Bartosik	Accelerator Physics