ISBN: 978-3-95450-192-2 doi:10.18429/JACoW-IBIC2017-TUPCF04

FEEDBACK CONTROLLER DEVELOPMENT FOR THE APS-MBA UPGRADE*

H. Bui†, D. Paskvan, A. Brill, S. Veseli, A. Pietryla, T. Fors, S. Shoaf, S. Xu, N. Sereno, R. Lill, N. Arnold, J. Carwardine, G. Decker

Advanced Photon Source, Argonne National Laboratory, Argonne, IL 60439, USA

Abstract

The Advanced Photon Source (APS) is currently in the preliminary design phase for the multi-bend achromat (MBA) lattice upgrade. Broadband Root Mean Square (rms) orbit motion should stay within 10% of a beam cross-section of the order 4 µm x 4 µm rms at the insertion device source-points. In order to meet these stringent AC beam stability requirements, a new orbit feedback system is under development and is being tested on the existing APS storage ring. The controller prototype uses Commercial Off-The-Shelf (COTS) hardware that has both high-performance Xilinx Field-Programmable Gate Array (FPGA) and two high-performance Texas-Instruments Digital Signal Processors (DSP) onboard. In this paper, we will discuss the rationale for a combined DSP/FPGA architecture and how functions are allocated. We then present the FPGA architecture and the results of using Infinite Impulse Response (IIR) filtering to mitigate Beam Position Monitor (BPM) switching noise and aliasing.

INTRODUCTION

The Feedback Controller (FBC) receives turn-by-turn (TbT or 271 kHz) BPM data from commercial Instrumentation Technologies Libera Brilliance+ BPM electronics [1], decodes and performs data integrity check, notifies the DSPs to generate corrector setpoints, and forwards corrector setpoints to the fast corrector power-supply interface.

Currently, the prototype Feedback Controller uses a CommAgility AMC-V7-2C6678 [2] module as a base development platform. The AMC-V7-2C6678 is a single width, mid-size Advanced Mezzanine Card (AMC), is comprised of two Texas Instrument (TI) TMS320C6678 DSPs, each with 8 cores running at 1.25 Giga Hertz (GHz), and a Xilinx Virtex-7 VX415T [3] FPGA. The combined architecture of a FPGA and a DSP shortens the development cycle time by taking full advantage of a vast library of highly-optimized DSP code and algorithms developed over the past 20 years for the present APS real-time feedback system (RTFB), which is running on a previous-generation of TI DSP. Investigations may be performed in the future to determine if any functionalities handled by the external DSPs can be implemented using resources inside the FPGA to improve system performance.

Figure 1 shows the simplified block diagram of the prototype FBC system. Light-blue blocks represent functionalities that are implemented inside the Virtex-7 FPGA, while orange blocks represent the two external TI DSP devices.

Xilinx FPGA's Gigabit transceivers and Peripheral Component Interconnect Express (PCIe) 2.0 are used to transfer data between the FPGA and DSP subsystem.

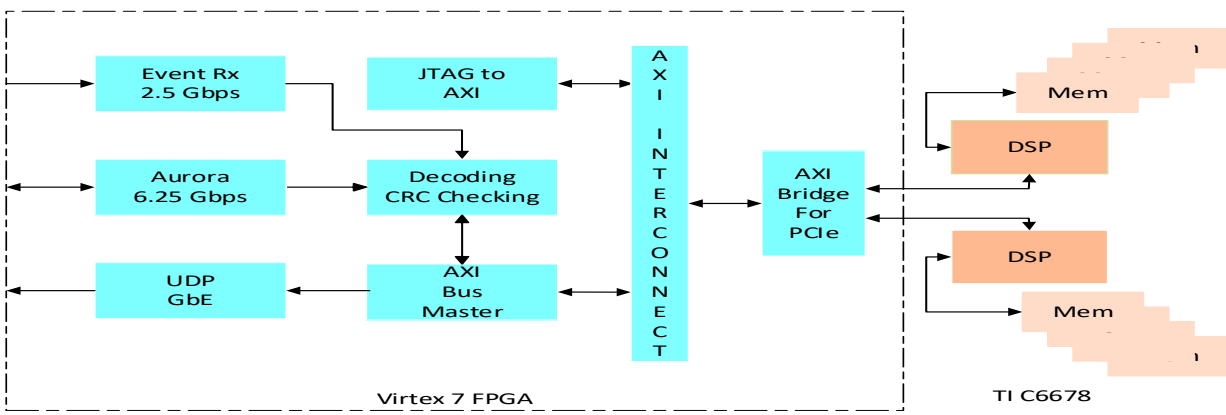

Figure 1: Simplified Block Diagram for the prototype FBC.

* Work supported by the U.S Department of Energy, Office of Science, under Contract No. DE-AC02-06CH11357
† hbui@aps.anl.gov

ISBN: 978-3-95450-192-2 doi:10.18429/JACoW-IBIC2017-TUPCF04

FPGA IMPLEMENTATION

The FBC Functional blocks implemented inside the FPGA are:

- Embedded Event Receiver
- Aurora 64b/66b
- UDP for GbE
- Data decoding and CRC checking
- AXI Bus Master
- AXI Interconnect
- AXI bridge for PCIe
- JTAG to AXI

Embedded Event Receiver

An Embedded Event Receiver, developed by Lawrence Berkeley National Laboratory (LBNL) re-targeted in a Xilinx Virtex-7 FPGA, receives the system timing serial events from a Micro Research Finland (MRF) timing system event generator over a 2.5 Gb/s fiber link. It decodes the events, provides timestamps, and generates trigger signals, which are synchronized with the machine clock. One of these trigger signals is called the 12th turn event, which is used to down sample TbT BPM data.

Aurora 64b/66b

An Aurora 64b/66b module uses standard 64b/66b encoding. It is a lightweight high-speed serial communication protocol for use with Xilinx gigabit transceivers. The prototype FBC uses four Libera Brilliance+ units (16 BPMs) across two sectors of the APS storage ring. Each Libera Brilliance+ can be configured to have up to four BPM modules and one Gigabit Data Exchange (GDX) module for streaming TbT data from the BPM modules. The FBC utilizes a Xilinx 6.25 Gb/s Aurora fiber link to receive 16 TbT BPM data packages from four daisy-chained Libera Brilliance+ GDX modules. The structure of a BPM package conforms to 16 by 32-bit data words; it consists of a programmable package identification (ID), BPM button amplitudes, calculated BPM horizontal and vertical positions, timestamps, status, and Cyclic Redundancy Check (CRC).

UDP for GbE

User Datagram Protocol (UDP) for Gigabit Ethernet (GbE) is implemented in the FPGA logic. LBNL provided modifications to their existing UDP implementation to assist the APS during development. In order to keep the transmission latency at a minimum, the UDP communication link is on a dedicated network using a cut-through switch. The FBC uses UDP to broadcast the 22.6 kHz corrector set points to the corrector power-supply controllers.

Data Decoding and CRC Checking

The Data decoding and CRC checking blocks perform data integrity and validity checks for every BPM data package received from the Aurora link. Incoming BPM data is decoded and sorted based on the pre-assigned package ID. The CRC for every package is re-computed then compared against the transmitted CRC value, and a CRC error is generated when there is a mismatch between the two CRC values. If the CRC is good, BPM data of the current package is selected and sent downstream for further processing, otherwise the previous saved valid data set will be sent instead.

AXI Interconnect

An Advanced eXtensible Interface (AXI) Interconnect is a Xilinx general-purpose core that provides connections for transferring data for any combination of AXI master and slave devices connected to an AXI Interconnect. It performs all the necessary conversions for any connected master and slave that have different data widths, clock domains, or AXI protocol.

AXI Bridge for PCIe

An AXI Bridge for PCIe is a Xilinx core that serves as an interface between the FPGA and DSPs using a Xilinx integrated block for PCIe. The PCIe interface is a two lane PCIe running at 5Gbaud/lane. The AXI Bridge for PCIe performs the address translations between the AXI memory space and PCIe memory space. The AXI Bridge allows the FPGA; configured as a PCIe endpoint; to perform Direct Memory Access (DMA) transactions between internal AXI connected peripherals and an external host device over the PCIe links.

AXI Bus Master

An AXI Bus Master module is implemented using the AXI4 protocol. It is an AXI memory mapped bus master capable of transferring a data burst up to 256 data beats, which can vary in size ranging from eight bits to 1024 bits, with a single start address. The AXI Bus Master waits for the 12th turn event from the Embedded Event Receiver and initiates an AXI burst write of BPM data with timestamps to the PCIe memory space. It then notifies the DSP to compute the corrector set points, waits for the DSP to indicate that new corrector set points are available, performs an AXI burst read from the PCIe memory space, and sends the corrector set points to the power supply controllers via UDP. Burst data transfers between the FPGA and the DSP are going across the AXI Bridge for PCIe.

JTAG to AXI

The Joint Test Action Group (JTAG) to AXI is a Xilinx core that acts as an AXI bus master. The JTAG to AXI generates AXI transactions by driving all the required AXI control signals to communicate to all the downstream slaves. The FBC uses the JTAG to AXI as a debugging tool. It provides a command line interface to hardware through which internal system memory can be easily accessed via a console.

ISBN: 978-3-95450-192-2 doi:10.18429/JACoW-IBIC2017-TUPCF04

DSP IMPLEMENTATION

The prototype FBC is currently using three out of the 16 available cores on the DSPs. Core 0's main function is to execute the real-time feedback algorithm. It consists of calculating corrector errors that is done by a matrix multiplication of the Inverse Response Matrix and the BPM errors. The corrector errors are then fed into the regulator, which consists of a high pass filter, low pass filter and Proportional Integral Derivative (PID) controller.

Core 0 of the DSP receives interrupts from the FPGA at the rate of 22.6 kHz. The FPGA writes BPM data into the DSP memory over PCIe bus and interrupts the DSP to generate new corrector set points. When the new corrector set points are available, the DSP generates an interrupt to the FPGA to read corrector set points from DSP memory over PCIe bus. The DSP takes approximately 11uS to execute the algorithm. In order to minimize execution time, other tasks are off loaded to core 1 and core 2. Core 1 performs the control and supervisory tasks. This core is responsible for receiving all control parameters and writing out collected data. Core 2 is the management core that handles all the communication between core 0 and core 1.

FILTER IMPLEMENTATION

The GDX module of the Libera Brilliance+ is equipped with a configurable Infinite Impulse Response (IIR) filters that can be applied to the TbT data stream for each BPM. The IIR implementation is a Direct Form II biquad, with a cascaded series of four biquads forming an eighth order IIR filter. Filter coefficients and gains are defined using Matlab's fdatool plugin. By choosing the desired characteristics of the filter, the fdatool generates the required filter coefficients to apply to the IIR for each BPM.

To improve long-term stability the Libera Brilliance+ uses ADC switching, which results in spikes at harmonics of 3.4 kHz. The FBC down samples TbT data to 22.6 kHz, which causes aliasing of signal above the Nyquist frequency of 11.3 kHz.

To mitigate the two noise sources, the filter we designed consists of second order notch filters for the first two switching harmonics, and a fourth order low pass filter with a cut-off frequency of 10 kHz for antialiasing. This was chosen as a compromise between antialiasing performance and group delay.

Figure 2 shows the antialiasing filter performance. It clearly shows that those spikes caused by aliasing higher switching harmonics are suppressed when the IIR filter is enabled.

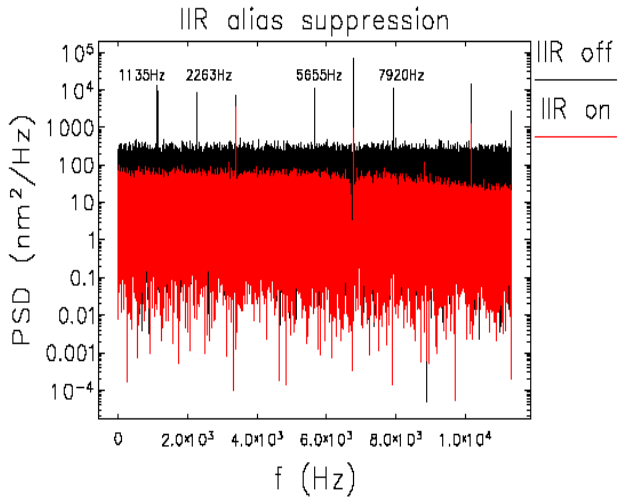

Figure 2: Antialiasing Filter Performance.

As the low pass cut off frequency is reduced, the group delay increases, reducing the orbit correction bandwidth of the FBC. Our fourth order low pass Butterworth filter has a group delay of 14 samples. A second order low pass Butterworth filter with a cut off frequency of 10 kHz reduces the group delay to six samples. Studies with beam revealed that the orbit correction bandwidth of the FBC is more sensitive to latency than to aliased noise. The system latency added by enabling the IIR filter reduces the orbit correction bandwidth of the FBC. More studies will be conducted to further investigate and improve filter performance.

CONCLUSION

The current architecture and technology used to develop the prototype Feedback Controller increases the feedback rate from 1.5 kHz to 22.6 kHz. First beam test results [4] and on-going integrated testing indicate that the prototype Feedback Controller is capable of achieving the stringent beam stability goals required for the APS upgrade.

ACKNOWLEDGMENT

The authors would like to thank Eric Norum and the LBNL team for their contributions to the development of the prototype Feedback Controller. We also would to thank all of the members of the APSU team.

REFERENCES

[1] Instrument Technologies, http://www.i-tech.si/accelerators-instrumentation/libera-brilliance-plus/benefits_1

[2] CommAgility Limited, https://www.commagility.com/products/hardware/435-amc-v7-2c6678

[3] Xilinx Inc., https://www.xilinx.com/products/silicon-devices/fpga/virtex-7.html

[4] N. S. Sereno *et al.*, "First Beam Tests of the APS MBA Upgrade Orbit Feedback Controller," in *Proc IBIC2016*, Barcelona, Spain, Sept. 2016, pp. 39 – 42.