An Intra Bunch Train Feedback System for the European XFEL

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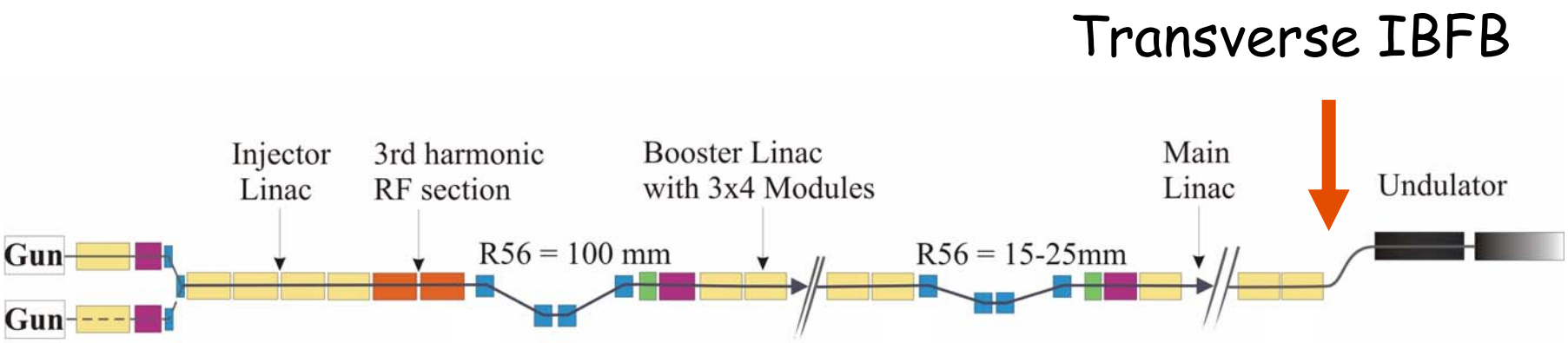
Project Background

- PSI/Switzerland & DESY proposed participation of PSI in beam stabilisation of the E-XFEL
- Spring 2004: PSI requests funding for prototype Intra-Bunchtrain Feedback System (IBFB)
- 12/2004: Swiss government signs MoU for participation in preparatory phase of E-XFEL & grants funding to PSI (for 3 years): 2.1 MCHF man-power
  1.6 MCHF hardware
- 3/2005: Technical contract PSI-DESY about IBFB & XFEL activities
- 7/2005: Recruitment of 4 people at PSI finished

Goal

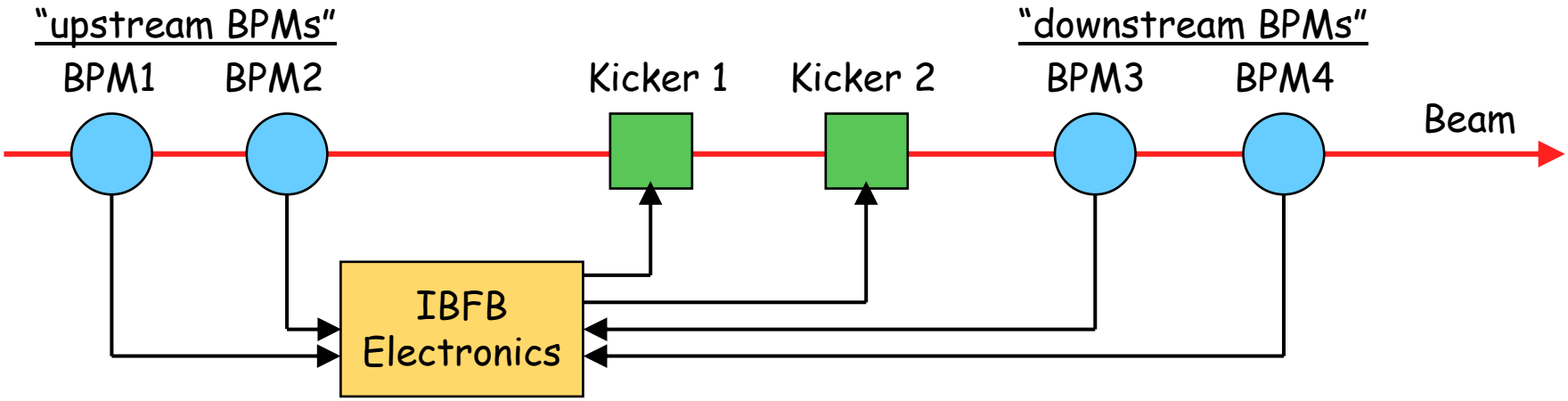
- IBFB prototype aims to achieve Sigma/10 ~ 3 µm transverse beam stability at E-XFEL undulator for stable SASE operation (-> BPM resolution ~ 1 µm)
- Relevant E-XFEL beam parameters:
  - ~20 GeV
  - 200 ns bunch spacing
  - ~30 µm transverse beam size
  - 1 nC, 80 fs
  - 3250 bunches in a train (650 µs)
  - Train rep. rate 10 Hz
- IBFB latency ideally < 200 ns: use measured positions of bunch no. N, N-1, N-2, ... to calculate & apply correction to bunch no. N+1

E-XFEL Layout



- Transverse IBFB: after main linac in front of switch yard
- Longitudinal IBFB: not discussed here, needs (much) more R & D (which monitors, which actuators, what needs to be stabilized where to which degree, ...)

IBFB Topology



- Use beam positions at upstream BPMs of bunch no. N, N-1, N-2, N-3,... to calculate kicks for bunch no. N+1 using a model (200 ns bunch spacing)
- Use downstream BPMs to check & correct model (less fast)
- Why upstream (not downstream) BPMs for fast feedback loop ?
  - Less latency (beam and cable signals travel in parallel)
  - -> Larger distance between BPMs -> better angle resol.

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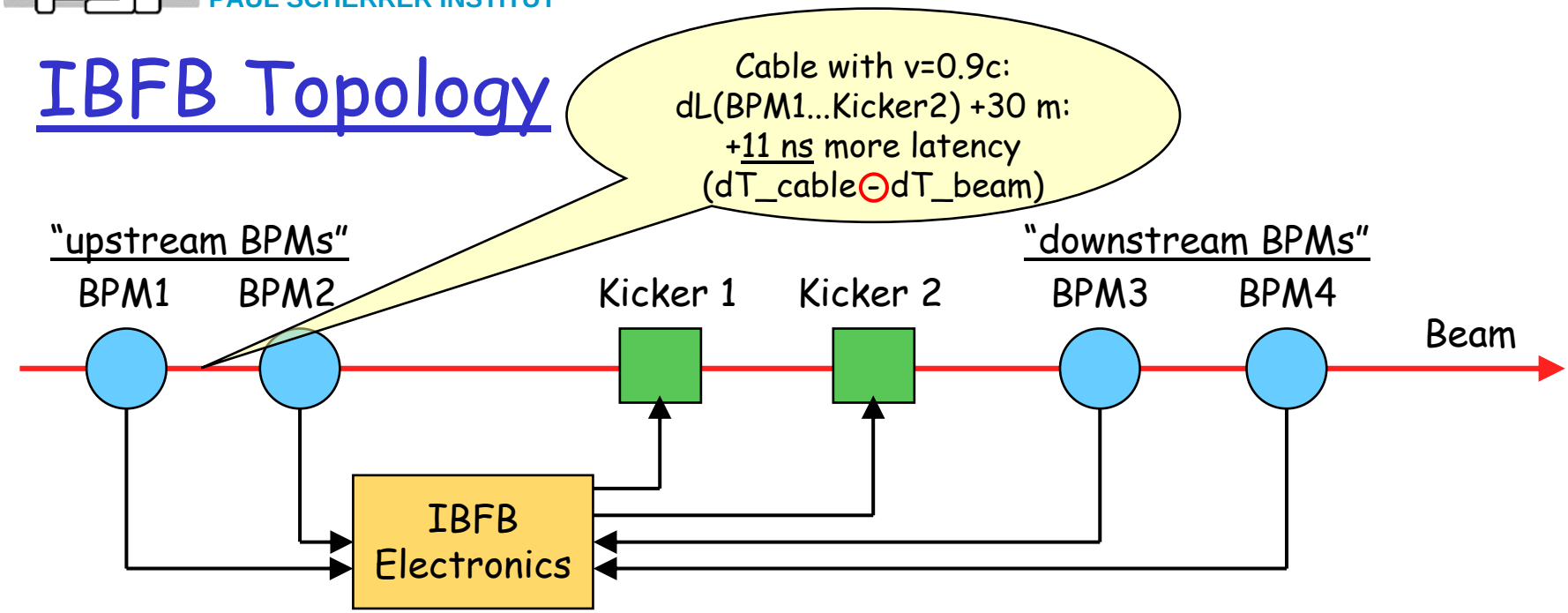

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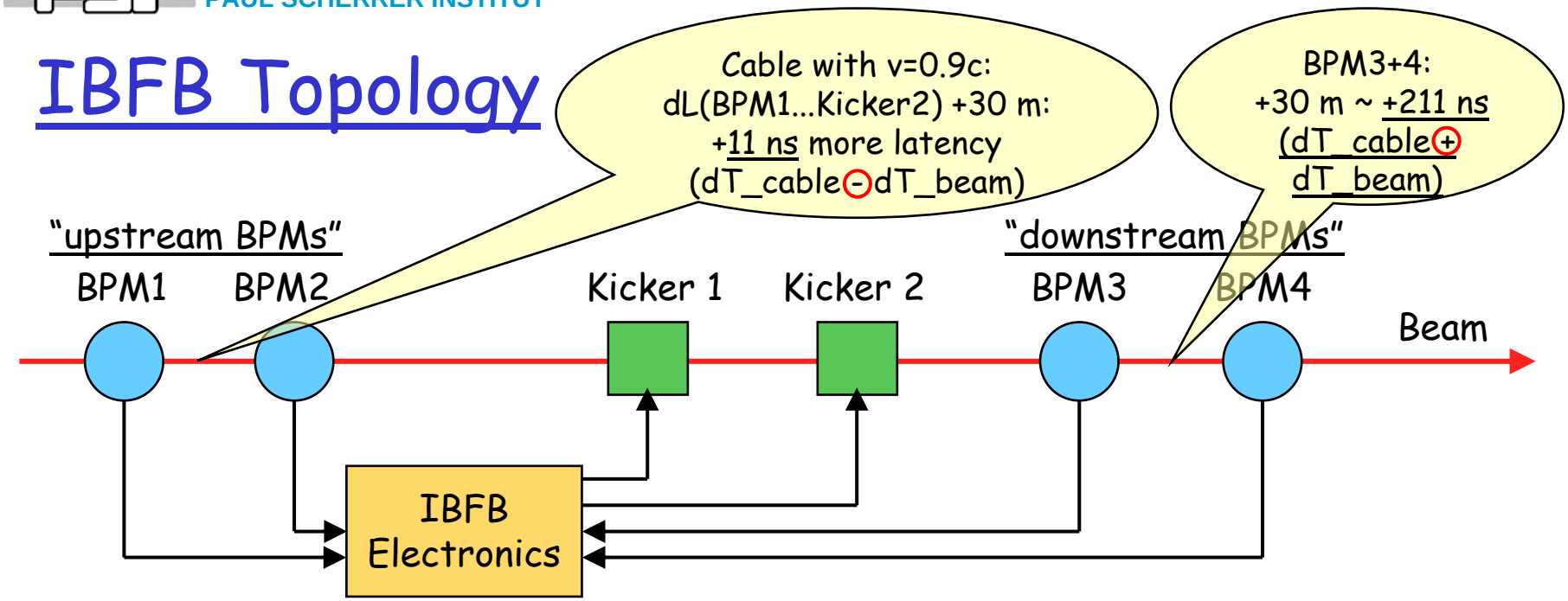

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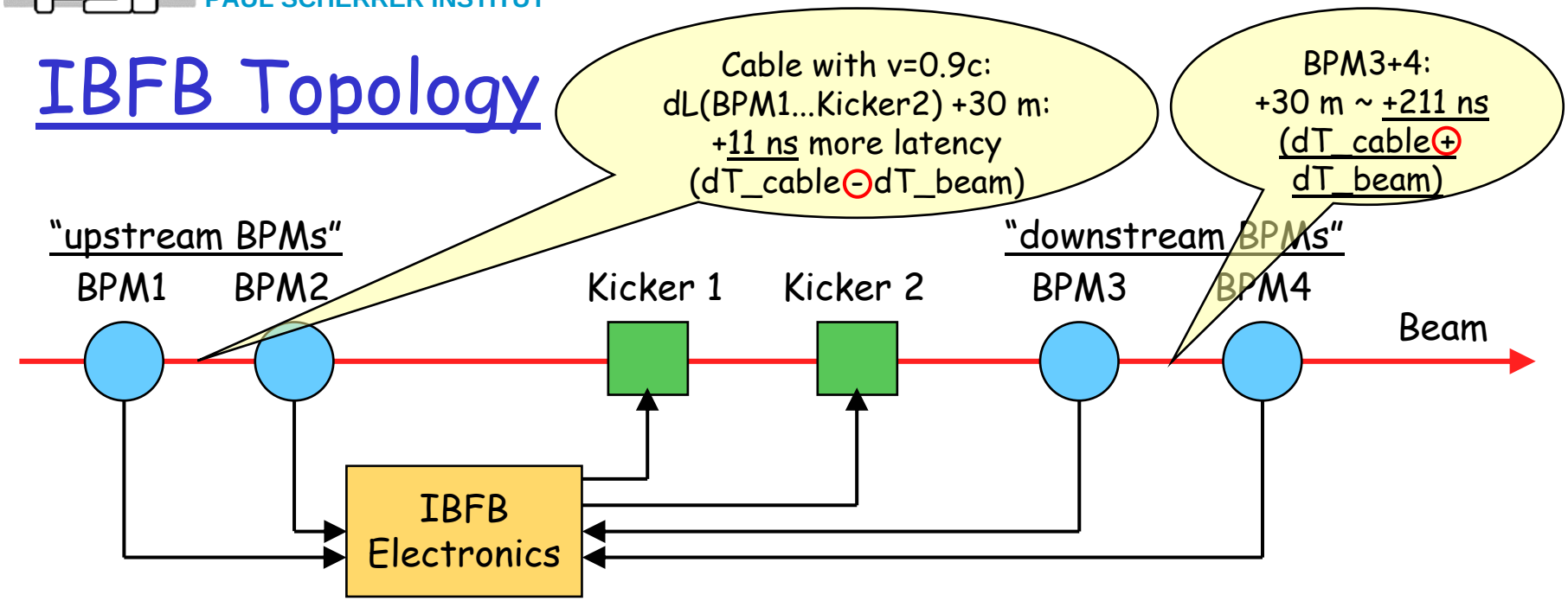

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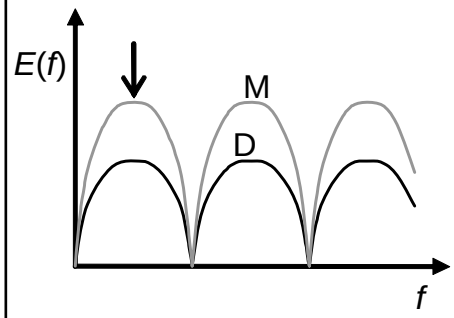
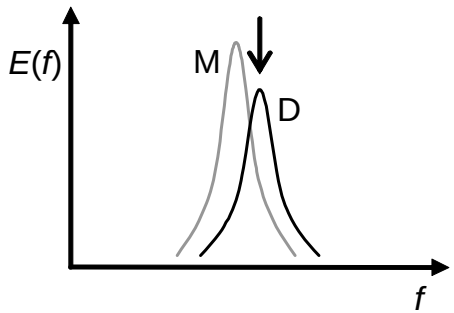
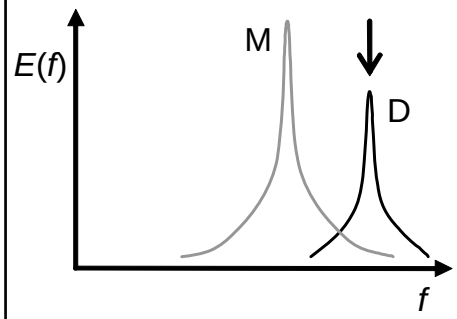
  - -> Larger distance between BPMs -> better angle resol.
  - BPM1+2 see unkicked beam: IBFB puts less noise onto the beam

IBFB Components

IBFB signal chain:	1st prototype	
• BPM pickups	5/2006	develop 1st
• RF-Front-End (RFFE)	7/2006	
• ADCs	11/2006	
• FPGAs/DSP/control system	11/2006	
• DACs	11/2006	
• Kicker Amplifiers	2006/2007	develop last
• Kickers	2006/2007	

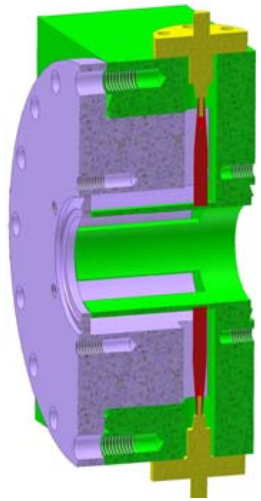
Development in-house at PSI, cooperation with DESY (BPM pickup construction, ...)

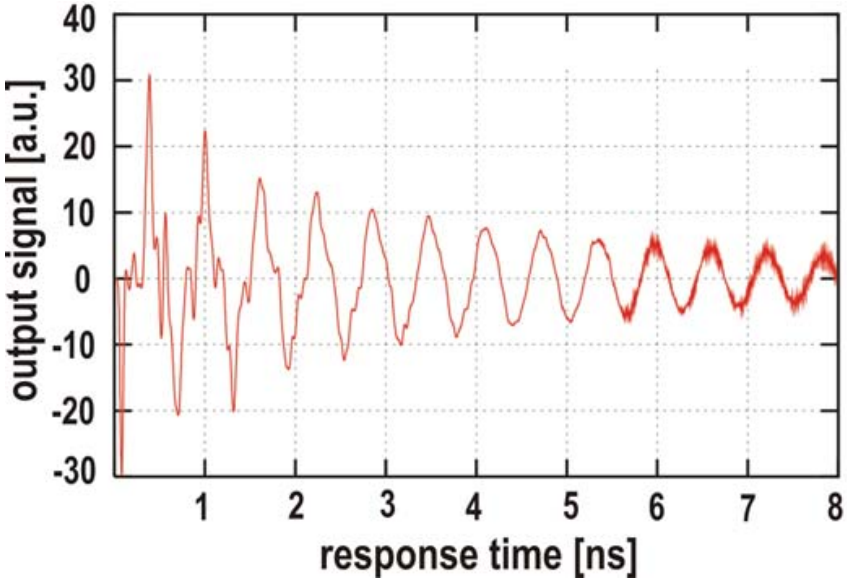
Choice of Pickup Type

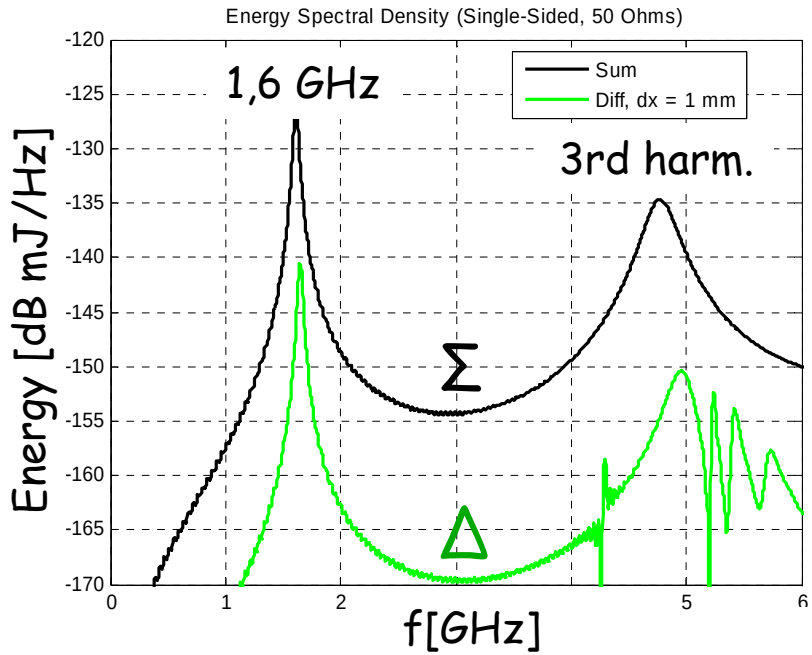
	Matched Stripline	Resonant Stripline	Cavity
Spectrum			
Application	DESY standard SL	IBFB-system ("working horse")	IBFB-system (study)
Frequencies	M: 375 MHz D: 375 MHz	M: 1610 MHz D: 1647 MHz	M: 3.4 GHz D: 4.3 GHz
Levels at 1nC, 1 µm, 50 MHz	M: -2 dBm D: -73 dBm	M: +20 dBm at f_D D: -47 dBm	M: ~ -60 dBm at f_D D: ~ -40 dBm
$Signal_D/Noise_{Th}$	24 dB	**50 dB**	**57 dB**
Pos. Offset	Mech., electr. proc.	Mech., electr. proc.	Mech., smallest

1.6 GHz Resonant Stripline BPM

- Q ~ 32, B ~ 50 MHz
- Sensitivity 2 mdB/µm
- EM design done (PSI, M. Dehler)
- Construction done (DESY, M. Siemens, S. Vilcins)
- Test: PSI lab 5/2006, SLS booster 8/2006
- "Working horse" BPM, to be tested at DESY FLASH

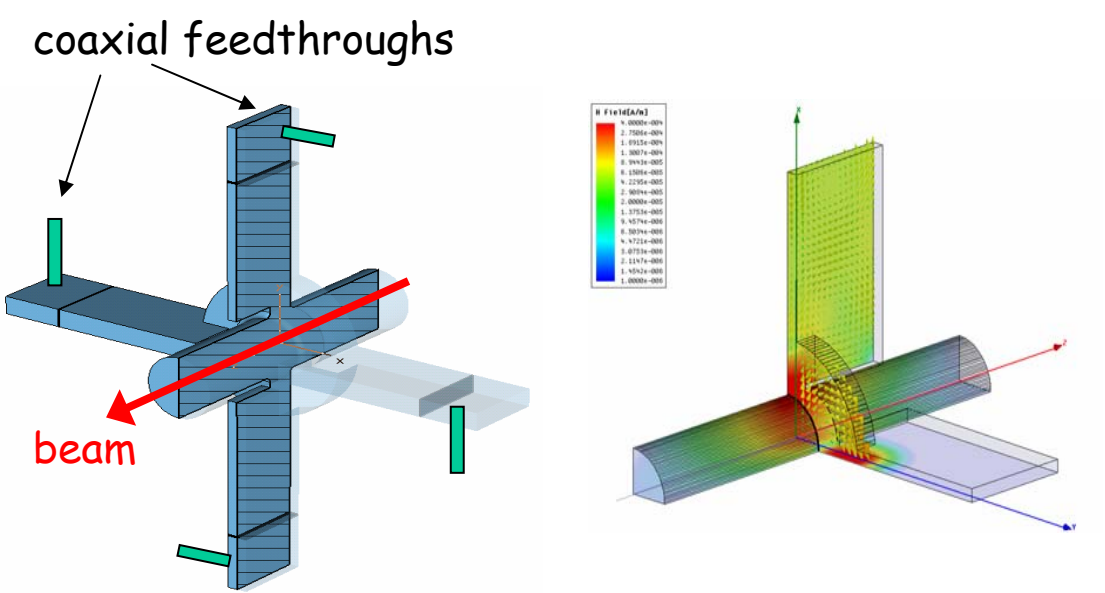




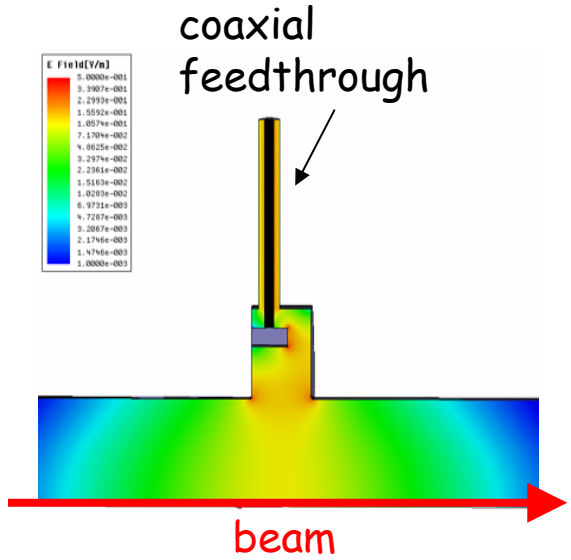


Cavity BPM

- R & D (improved resolution)
- 1 Position cavity: 4.3875 GHz dipole, loaded Q ~ 200
- 1 Reference cavity: 4.3896 GHz, Q ~ 120
- EM design done (PSI, A. Lounine)
- Construction drawings 5/2006, manufacturing 10/2006



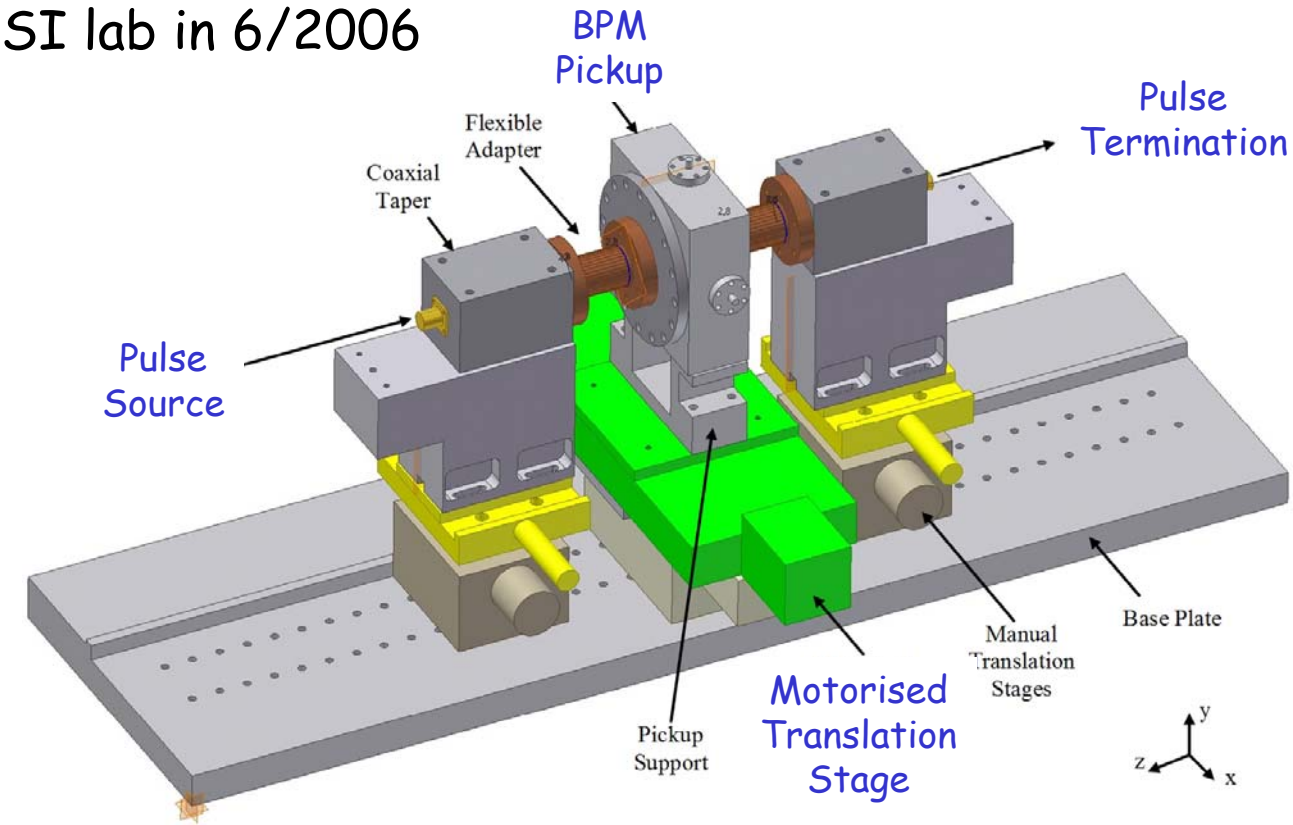
"Position" cavity (dipole TM11 mode but **no monopole TM01 mode coupling to waveguide**)



"Reference" cavity (upper half)

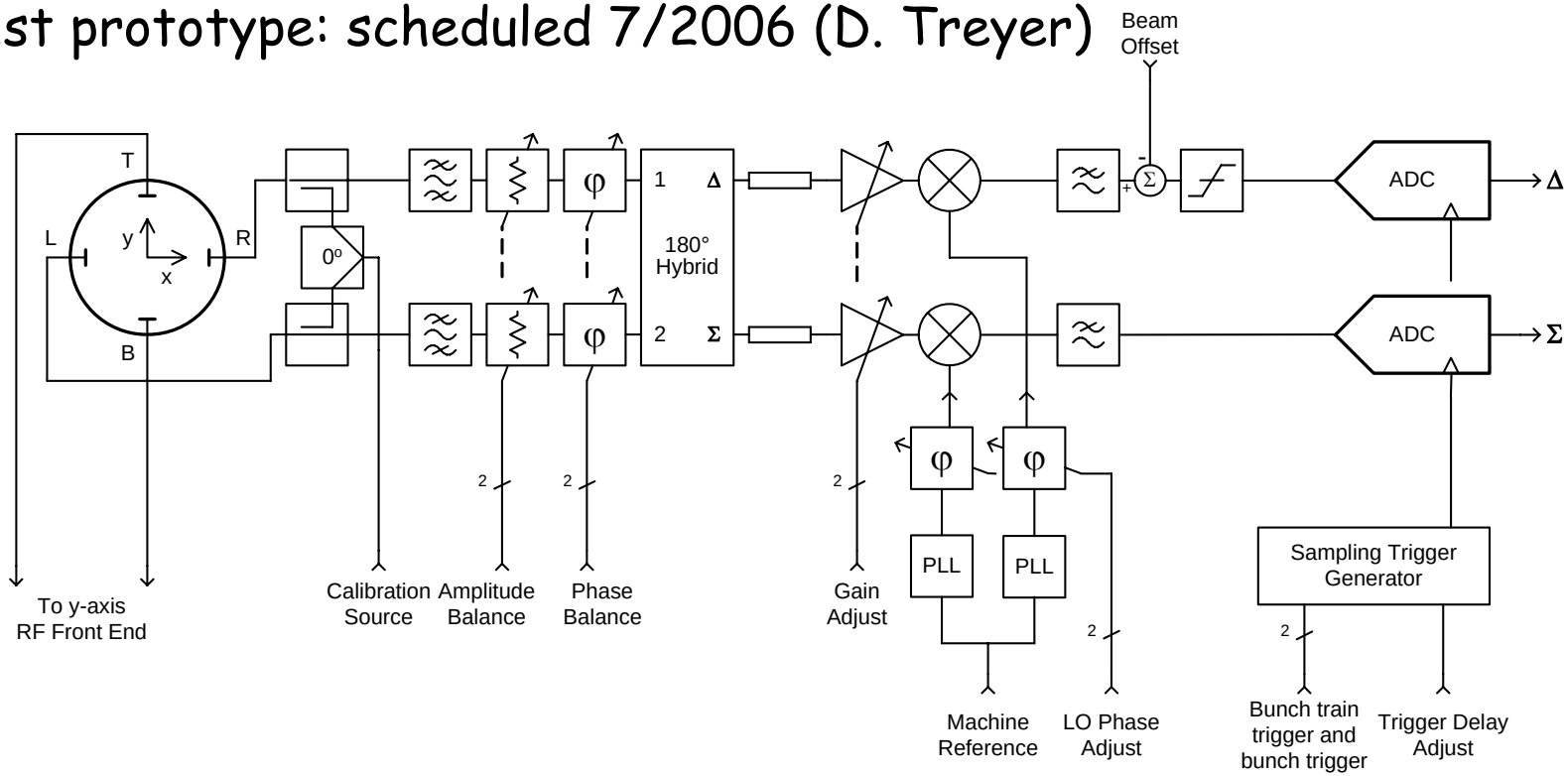
BPM Pickup Test Bench

- Simulates electron beam: pulse source, tapered coaxial line through BPM, position change via motors
- Used to characterise Pickups/RFFE/ADC before beam tests at SLS booster & DESY FLASH (automatic measurement, EPICS)
- Ready at PSI lab in 6/2006

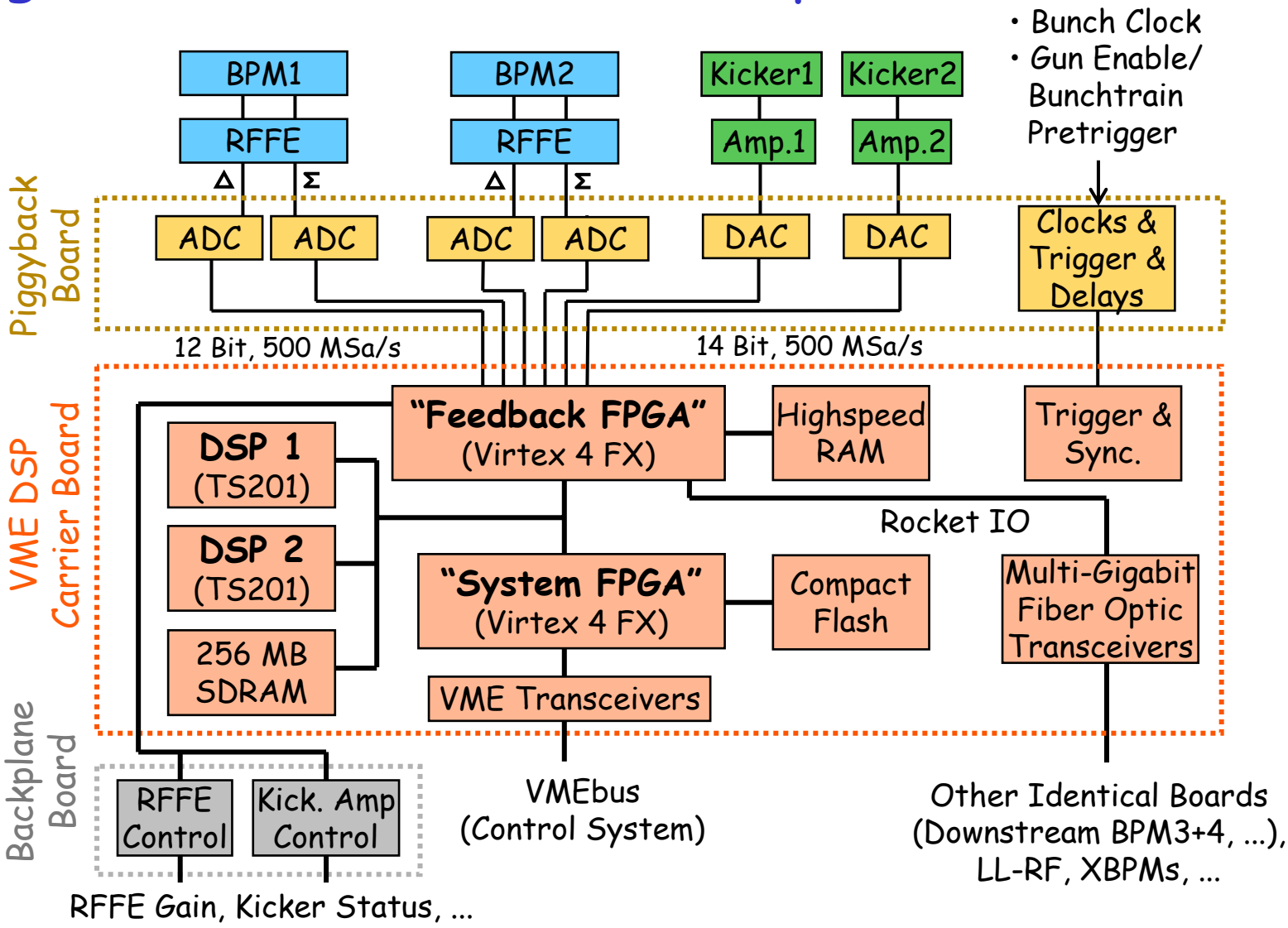


RF Front-End (1.6 GHz Stripline Pickup)

- Delta/Sigma via hybrid, mixed to (nearly) DC via multiplied bunch clock, sampled by 500 MSa/s ADC, online calibration (pilot source)
- Goal: 1 µm resolution (1 nC), < 30 ns latency, +- 500 µm range, +- 2.5 mm offset adjustment
- 1st prototype: scheduled 7/2006 (D. Treyer)



Digital IBFB Hardware Concept



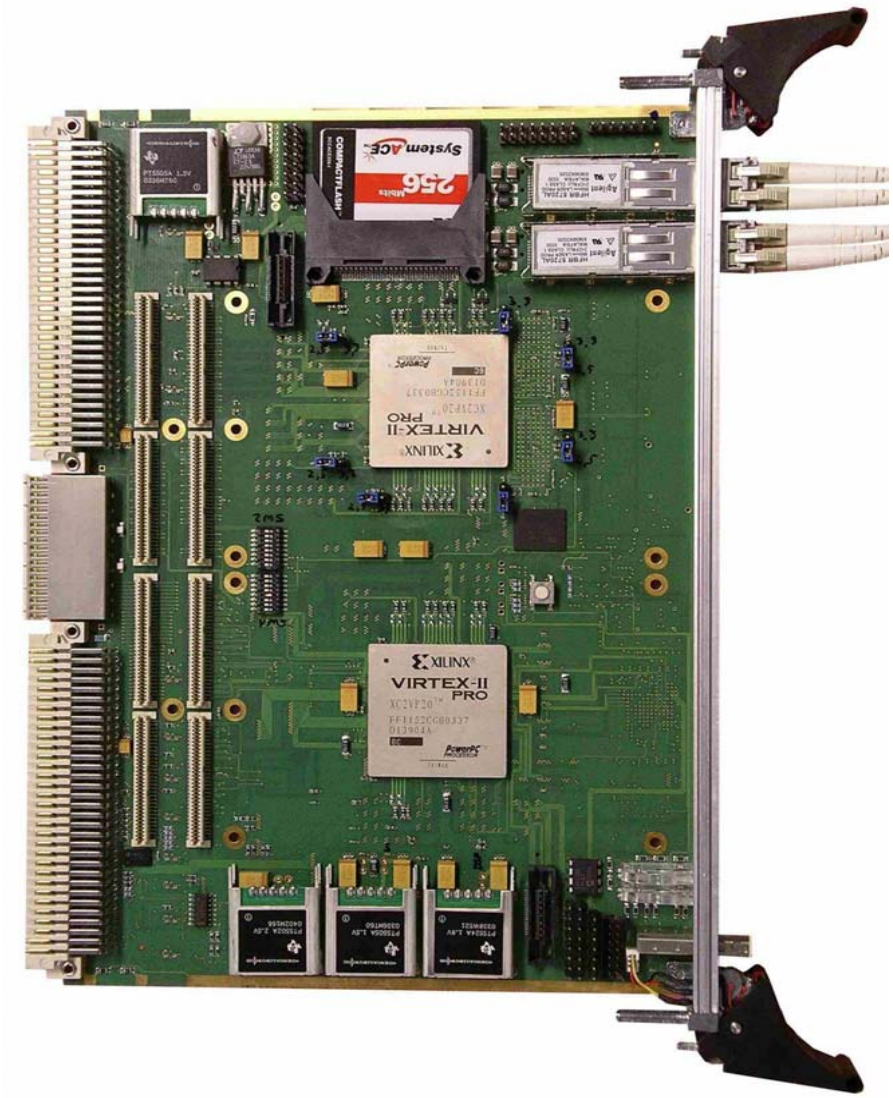
Digital IBFB Hardware Concept (Cont'd)

- Schedule: 1st Prototype 11/2006

- VMEbus carrier board: will be based on existing "VPC" board (licensed to company MEN) : re-use many parts of schematics & FPGA firmware (VME interface, Gigabit Links, ...)

- Other possible applications at PSI (SLS, proton accelerators, low emittance gun project, ...) -> synergy effects of IBFB and (future) PSI applications

- ADC/FPGA: Atmel 12-bit 500 MSa/s, demo board with interface to Virtex4FX FPGA ready 6/2006 -> Used to characterise RFFE



IBFB Algorithm

FPGA (VHDL): "Feedback" (Bunch-to-Bunch)

- Calculate positions (const.*Δ/Σ+offset) for bunch N
- Calculate theoretical "ideal" kicks that would be needed to correct bunch N (decoupling matrix, beam optics model)
- Calculate real kicks (DAC values) for bunch N+1, FIR filter as a predictor (using "ideal" kicks for bunches no. N, N-1, N-2, N-3, ...)
- Latency < 100 ns

DSP (C Code): Adaptive Feed-Forward (Bunchtrain-to-Bunchtrain)

- Determine systematic beam position perturbations (same for each bunchtrain)
- Provide & update lookup-tables for FPGA: adaptive feed-forward
- Check & adapt model used by FPGA (optics, kicker scaling, ...)
- Detect time-dependent model errors (energy chirp, ...): calculate & update table with bunch-no.-dependent model corrections for FPGA

Summary & Outlook

- 1.6 GHz resonant stripline pickup:
  - Lab tests on BPM test bench 5-7/2006
  - Installation of 3 BPMs at SLS booster 7/2006: noise correlation (0.5 nC, 1 µs bunch spacing -> like FLASH linac)
  - Installation of 4 BPMs at DESY FLASH linac 10/2006
- Cavity BPM:
  - Lab tests 2006/2007
- RFFE:
  - Lab test (12-bit 500 MSa/s ADC & Virtex4FX) 6-7/2006
  - Test at SLS booster 8/2006
  - Test at FLASH linac until end 2006
- VME FPGA/DSP board & ADC/DAC piggyback:
  - Working prototype end 2006
- Overall IBFB system integration & test (2007):
  - First IBFB tests at FLASH using existing kicker & amplifier
  - Design of kicker & amplifier for XFEL (20 GeV, ...)