

# Trends in fast feedback R&D

Alessandro Drago  
INFN-LNF

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on High Luminosity  $e^+e^-$  Factories**

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# Main topics

- Generality on fast bunch-by-bunch feedback systems
- Technology trends, DSP and FPGA
- Simulators
- Dafne feedback systems
- iGp feedback system upgrade
- Grow – damp measurements
- Tune spread measurements
- Conclusions

# Basic equation

- The  $n$ -th bunch can be described as an individual harmonic oscillator moving rigidly in the longitudinal plane (energy oscillations), or in the transverse (betatron) X, Y planes according to the equation. **In the longitudinal plane the dynamics is described by the following equation:**

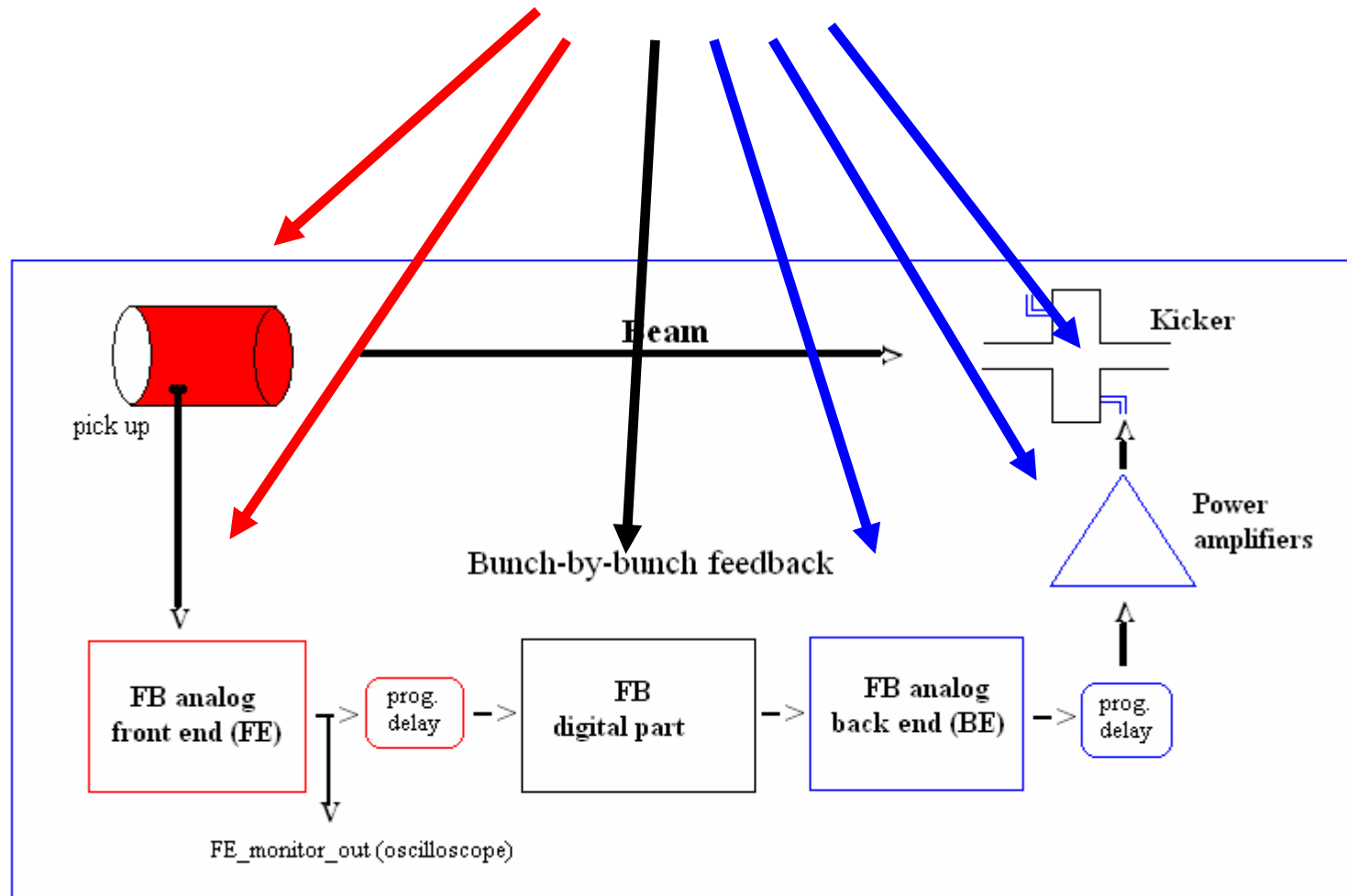
$$\ddot{\tau}_n + 2d_r \dot{\tau}_n + \omega_s^2 \tau_n = -\frac{\alpha_c e}{E_0 T_0} V_n^{\text{wk}}(t), \quad (1)$$

- where  $\tau_n$  is the arrival time (time delay) of the  $n$ -th bunch relative to the synchronous particle,  $d_r$  is the natural radiation damping,  $\omega_s$  is the natural (synchrotron) oscillation frequency,  $\alpha_c$  is the momentum compaction,  $E_0$  is the nominal energy, and  $eV_n^{\text{wk}}(t)/T_0$  is the rate of energy loss due to the superposition of the wake forces of the other bunches.
- The action of the feedback consists of individual kicks to each bunch increasing the damping term  $d_r$ . In the presence of an active feedback Eq. (1) becomes:

$$\ddot{\tau}_n + 2d_r \dot{\tau}_n + \omega_s^2 \tau_n = \frac{\alpha_c e}{E_0 T_0} [V_n^{\text{fb}}(t) - V_n^{\text{wk}}(t)], \quad (2)$$

- where  $V_n^{\text{fb}}(t)$  is the feedback kick given to the bunch  $n$ -th.

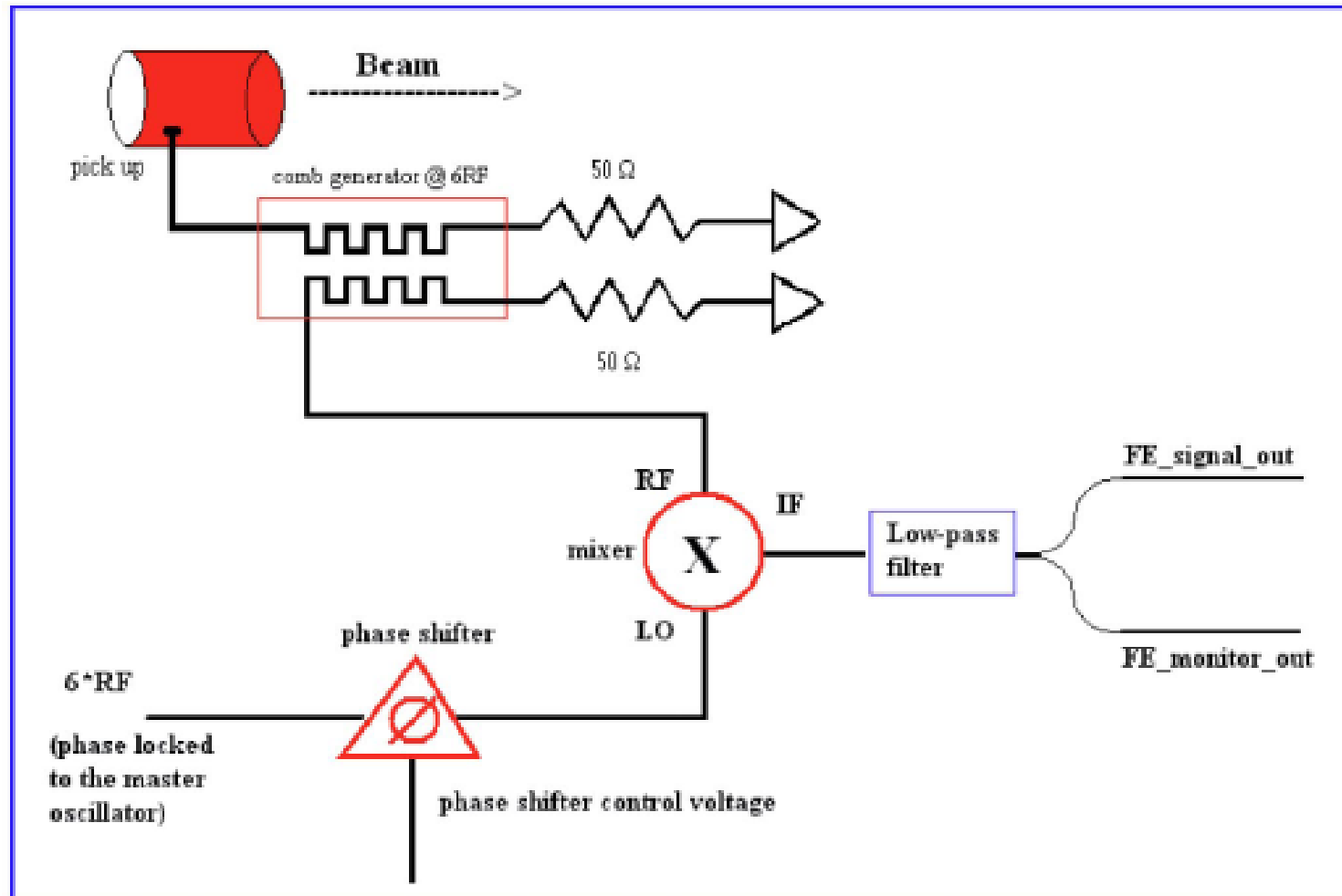
# Fast Feedback R&D



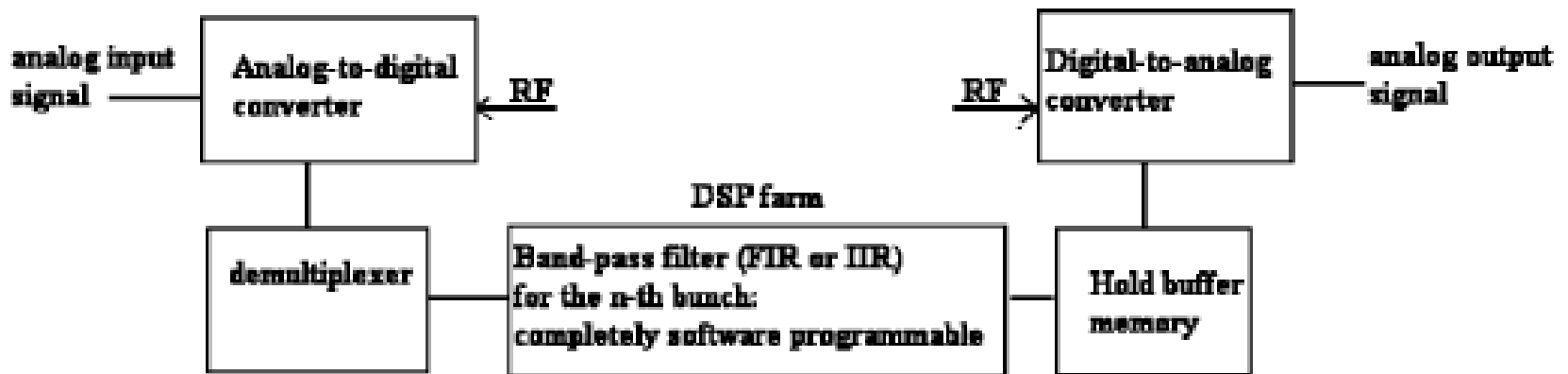
# LFB main blocks

- The LFB system consists of three main blocks:
- (i) An analog front end followed by a programmable delay, to detect the error signal of each bunch. The function of the programmable delay is to synchronize the output signal of this block with the digital part.
- (ii) A digital part, to manage separately the signal of every bunch with individual passband filters having a convenient gain and phase response. The global phase response of the feedback must give a 90 degrees phase shift at the dipole frequency.
- (iii) An analog back end (BE) followed by a second programmable delay, power amplifiers, and cavity kicker. The BE programmable delay has the task of synchronizing the peak of the  $n$ -th kick with the passage of the  $n$ -th bunch through the kicker.

# Front end (FE) block in DAFNE LFB



- In the digital part , the FE\_signal\_out is sampled by an A/D converter at rf frequency, and then demultiplexed to separate the signal of each bunch.
- A digital signal processor (DSP) farm is used to implement a passband filter [finite impulse response (FIR) or infinite impulse response (IIR)]. The number of taps, gain with sign, center frequency, filter shape, and phase response are programmable by the users, but the loaded filters have to be equal for all the bunches, even if it is possible to run an “exception” filter for just one bunch.



# IIR versus FIR bandpass filter

General form of **IIR filter** (infinite impulse response)

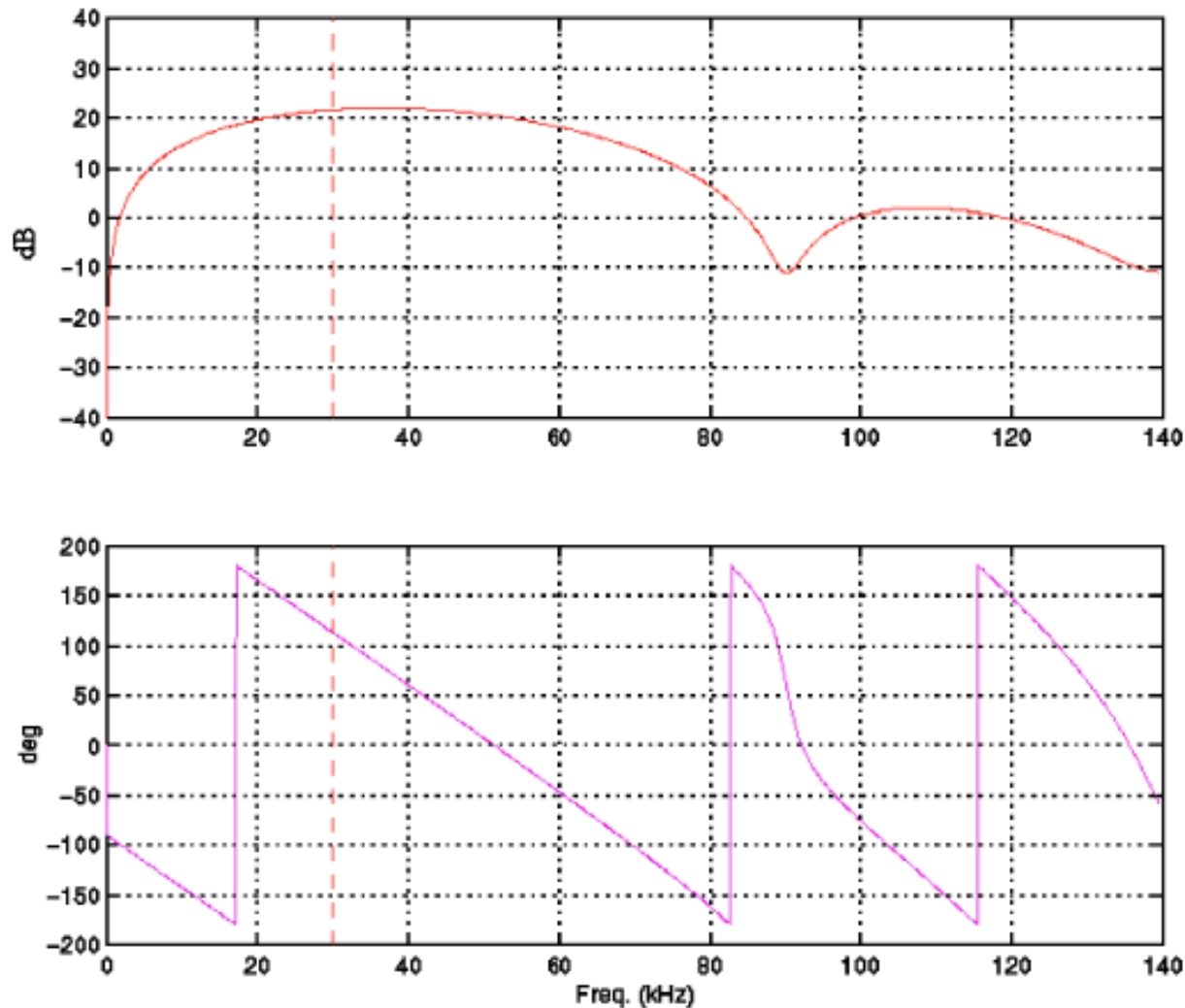
$$y_n = \sum_{k=1}^N a_k y_{n-k} + \sum_{k=0}^M b_k x_{n-k}$$

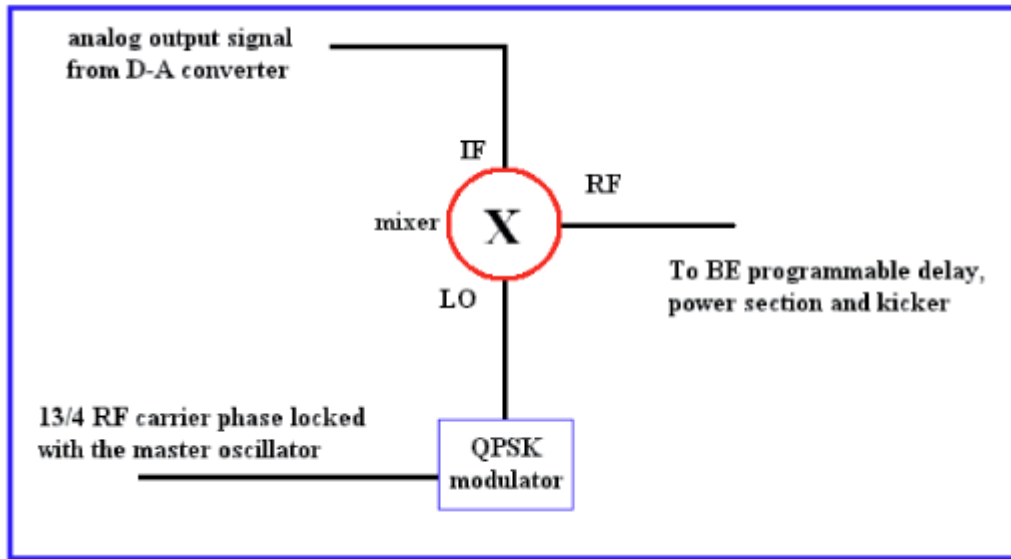
General form of **FIR filter** (finite impulse response)

$$y_n = \sum_{k=0}^M b_k x_{n-k}$$



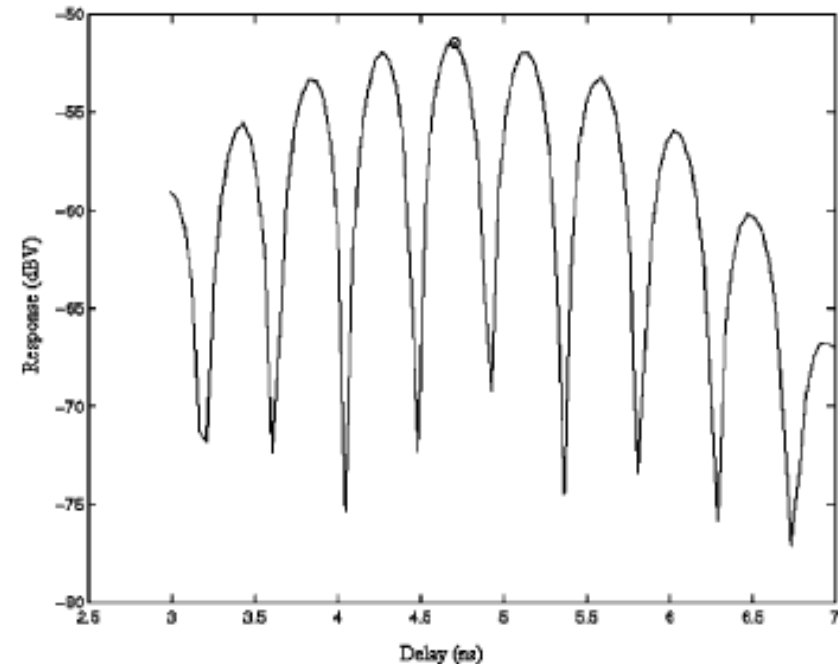
Amplitude and phase response versus frequency of a FIR filter implemented in the DSP farm for high current electron beams. Synchrotron frequency is by dotted line.





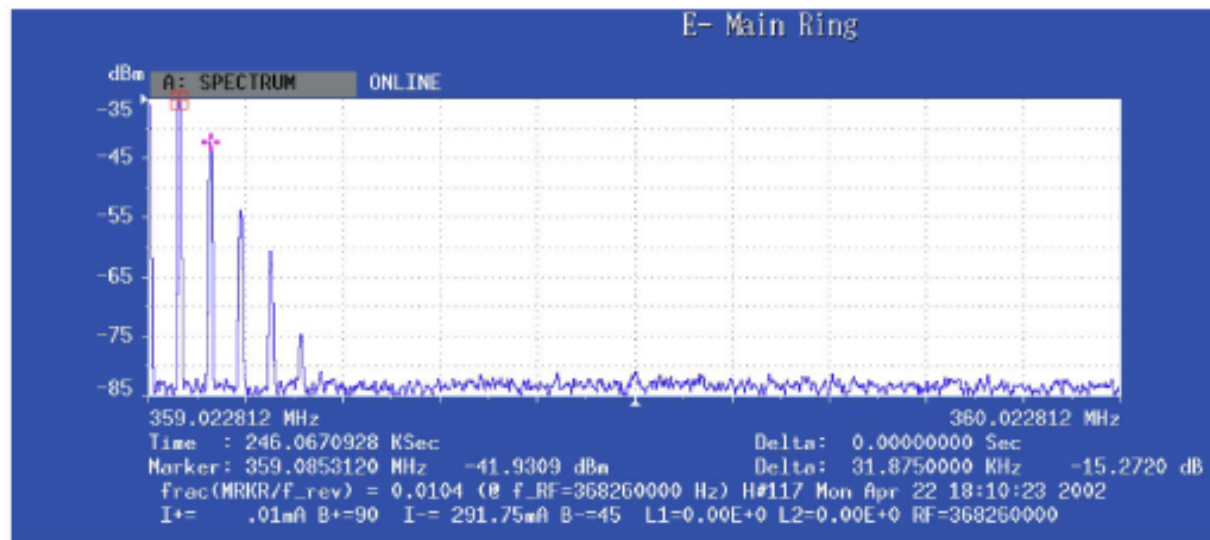
Longitudinal back-end response (dBV) versus BE programmable delay (ns).

Back end (BE) block in the DAFNE LFB system. This block has to adapt conveniently the DAC output to the power amplifier section

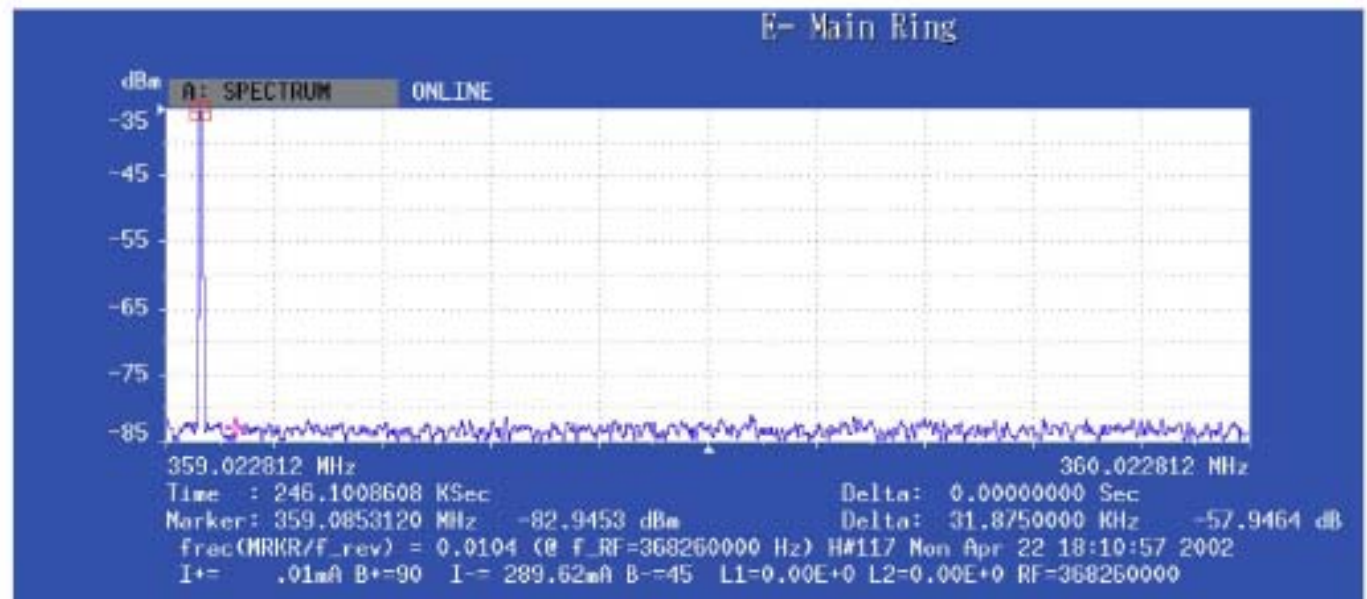


# E- Main Ring

Multibunch beam power spectrum at 300 mA with LFB off. The square marker is on the revolution harmonic; the cross marker is on the dipole oscillation right sideband.



Multibunch beam power spectrum at 300 mA with LFB on. The square marker is on the revolution harmonic.



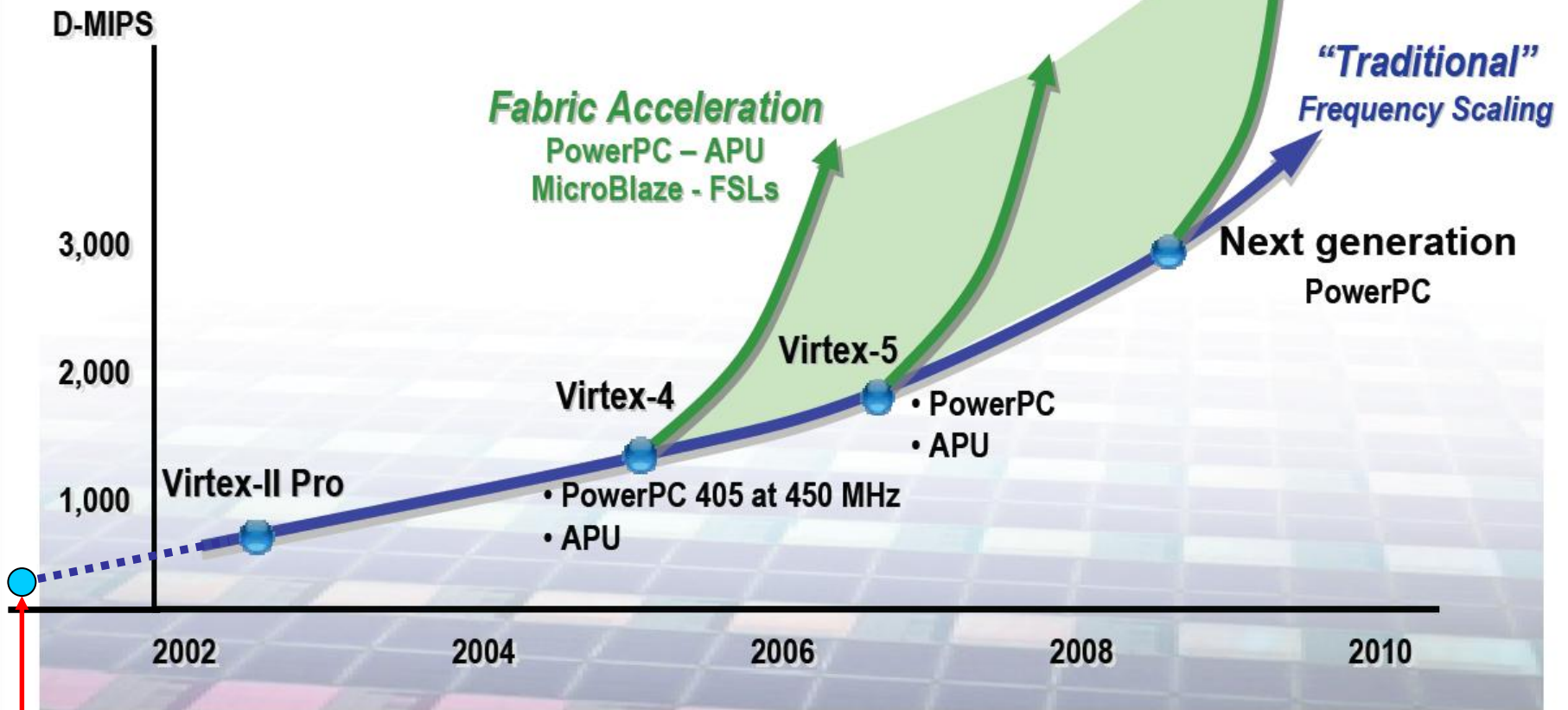
# Digital processing

- As well known, in the last 30 years huge progress have been done in the digital electronics
- DSP (digital signal processor) units are single chip microprocessors invented during mid-80's to process mainly voice and audio signals (.1-10kHz bandwidth)
- DSP units have dedicated instruction set to perform real time (but at low frequency) signal processing
- In the 90's a SLAC-ALS-LNF collaboration has built a bunch by bunch longitudinal system (still used!) with up to 80 DSP units working in parallel
- In DAFNE this LFB system can process signals up to ~50kHz

# The FPGA advent

- In the second half of 90's a new powerful technological step: the FPGA (field programmable gate array) units have put on the market
- FPGA are digital components with extremely high number of circuits in a single chip and the possibility to be reprogrammed "on the field" any time is necessary
- FPGA became so powerful to begin to include DSP units and PowerPc inside

# Processor Performance and Fabric Acceleration



2001  
VIRTEX-II

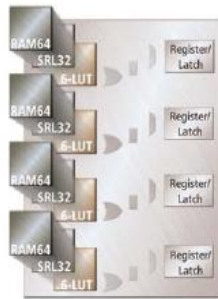
# Xilinx Virtex-5 performances

## 65nm ExpressFabric™ Technology

LX LXT SXT

Achieve highest performance, most efficient utilization on 65nm triple-oxide process

- 30% higher speed, 35% lower dynamic power, and 45% less area than the previous generation
- Industry's first LUT with six independent inputs for fewer logic levels
- Flexible LUTs are configurable as logic, distributed RAM or shift registers
- Advanced diagonally symmetric interconnect enables shortest, fastest routing
- From 30,000 to 330,000 logic cells for system-level integration

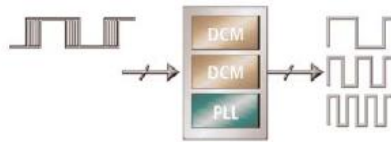


## 550 MHz Clocking Technology

LX LXT SXT

Achieve highest speeds with high-precision, low-jitter clocking

- 12 DCMs provide phase control of less than 30 ps for better design margin
- 6 PLLs reduce reference clock jitter by more than 2x
- Differential global clocking ensures low skew and jitter



## The Right Memory for Any Application

LX LXT SXT

Distributed RAM—Small

- Build 256-bit memory per CLB
- 64 bits per LUT

550 MHz, 36 Kbit Block RAM—Medium

- Configure Block RAM as multi-rate FIFO
- Built-in ECC for high-reliability systems
- Automatic power conservation circuitry

High-Performance External Memories—Large

- ChipSync™ technology for reliable interfaces
- Achieve data rates up to 389 Gbps

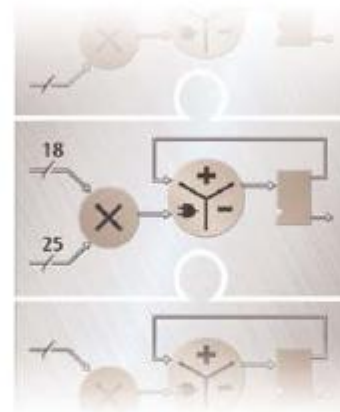


## 550 MHz DSP48E slice

LX LXT SXT

Achieve up to 352 GMACS DSP Performance

- Up to 640 DSP48E slices in Virtex-5 SX95T device
- Enhanced slice with 25 x 18 multiplier and 48-bit adder enables single-precision floating-point math and wide filters with fewer slices
- Configurable for DSP, arithmetic, and bit-wise logic
- Enables efficient adder-chain architectures
- 40% lower power consumption: 1.38mW/100MHz at a 38% toggle rate





# Using MATLAB and SIMULINK, the real time code can be easily integrated with the simulator code !



## Xilinx System Generator for DSP

42

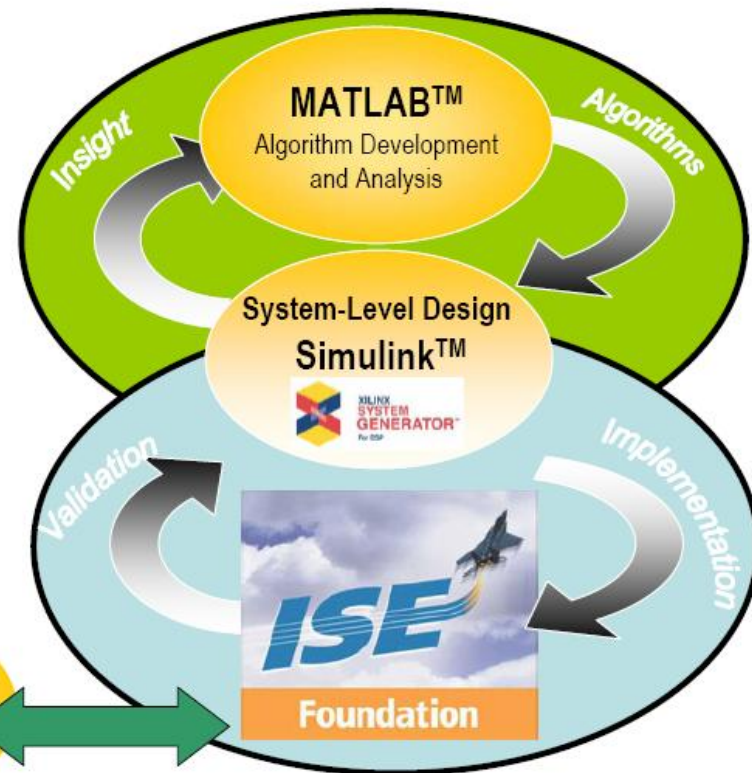
*Enabling success from the center of technology™*

### ■ System Generator for DSP

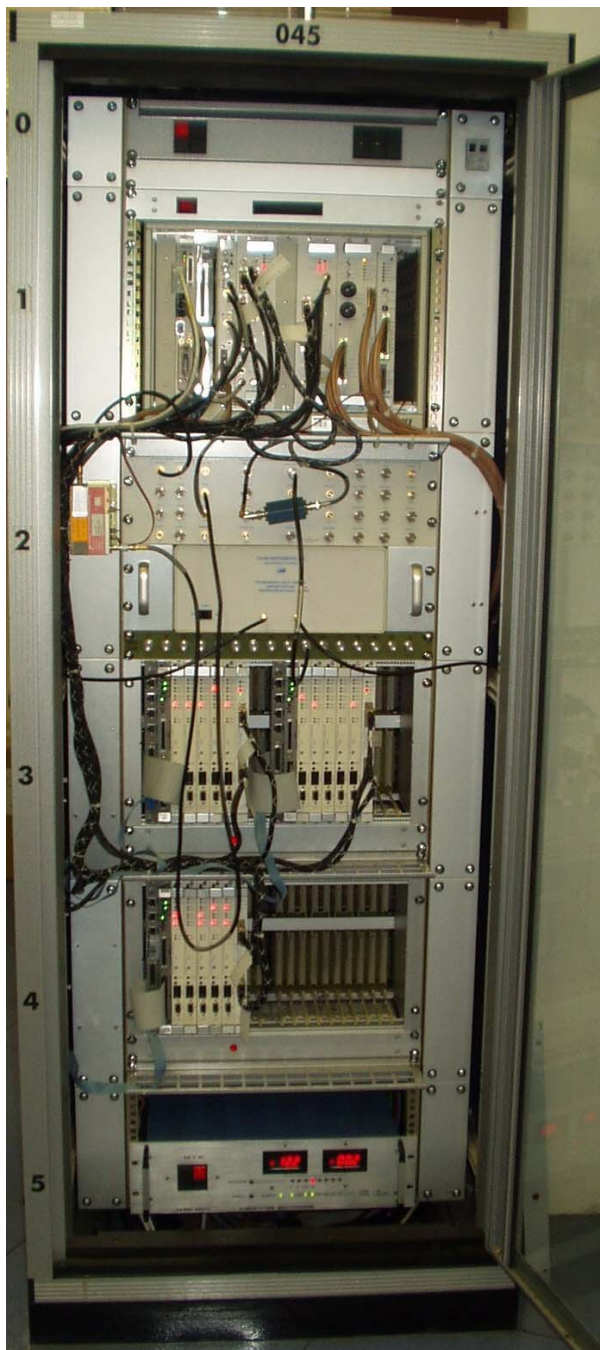
- Tightly integrated with MATLAB and ISE 8.2i
- IP Toolbox plug-in for simulink
- Full hardware design and simulation



3<sup>rd</sup> party prototype  
and development  
boards





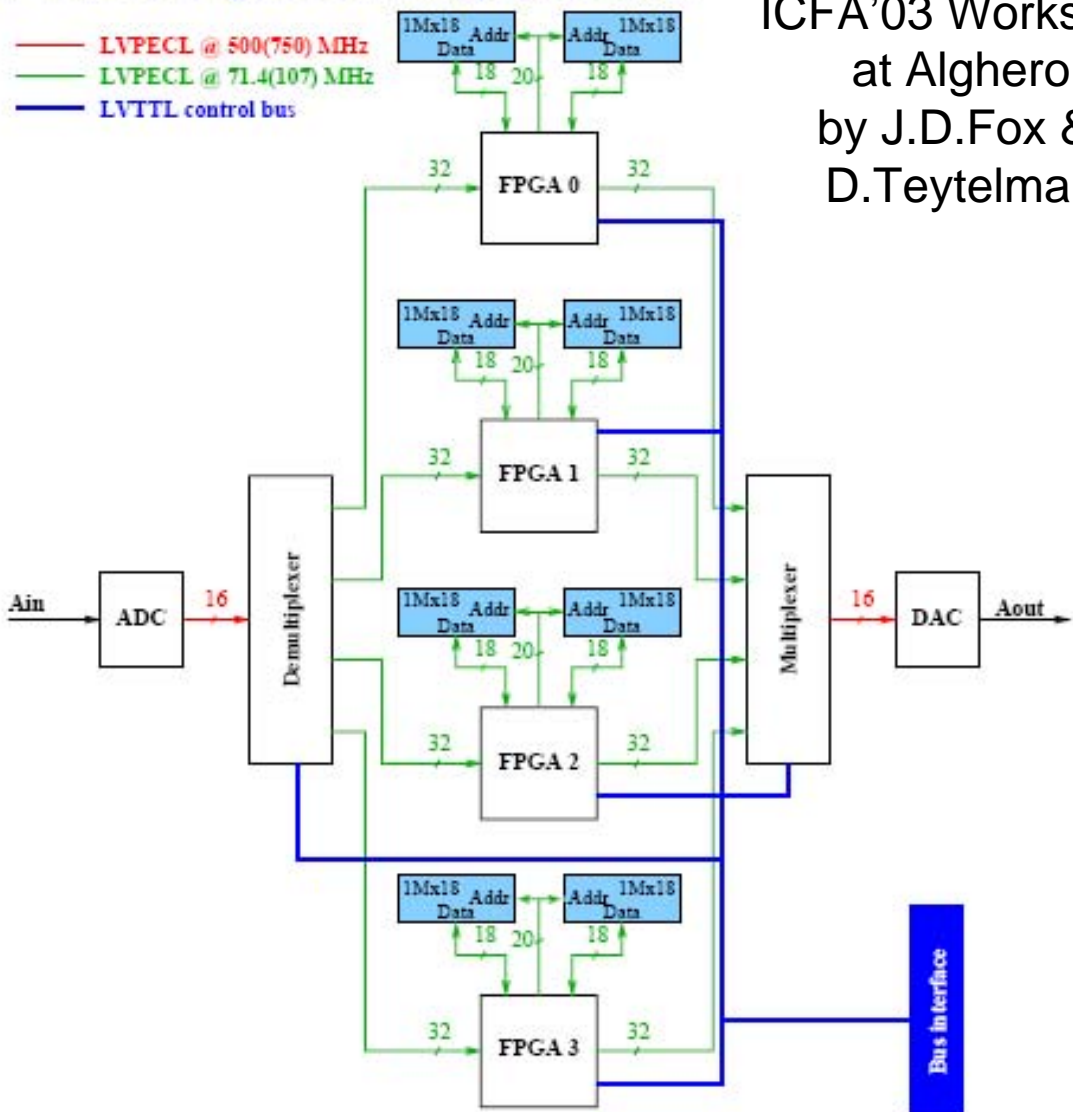


# Looking back: the first FB collaboration

- This is the longitudinal feedback developed in the years 1992-1996 by a SLAC – LBNL - LNF collaboration
- Still working @ PEP-II, DAFNE, ALS
- Four VME crate: each VME board contains 4 dsp
- The system can manage up to 80 dsp
- Each dsp can elaborate up to 32 bunches.

## GBoard 1.5 GS/sec. processing channel

- Next-generation instability control technology
- SLAC, KEK, LNF-INFN collaboration - useful at PEP-II, KEKB, DAFNE and several light sources.
- Transverse instability control
- Longitudinal instability control
- High-speed beam diagnostics (1.5 GS/sec. sampling/throughput rate)
- Builds on existing program in instability control and beam diagnostics.
- Significant advance in the processing speed and density previously achieved.



Presented at the  
ICFA'03 Workshop  
at Alghero  
by J.D.Fox &  
D.Teytelman

# iGp (integrated Gigasample processor) feedback collaboration

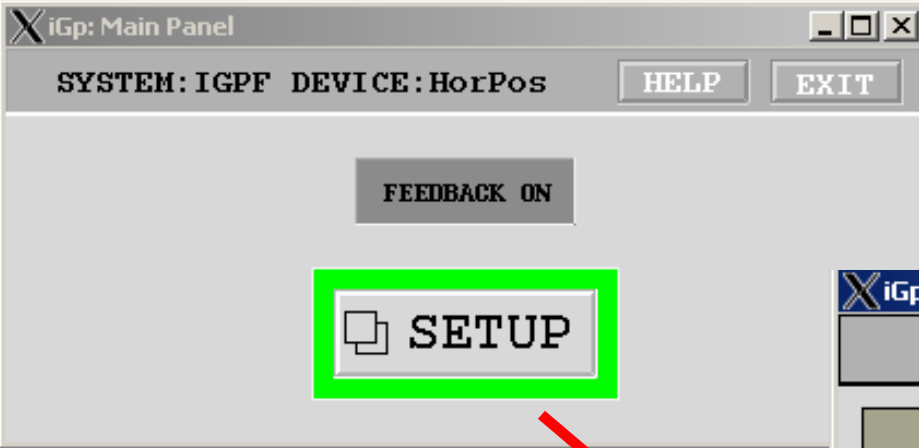
- The iGp system has been developed by a collaboration of KEK-SLAC-LNF starting around 2002-2003 as a "small" **test system** for the "big" Gboard feedback system.
- The iGp feedback system is a baseband bunch-by-bunch signal processing channel designed around a **single** Virtex-II FPGA by Xilinx.
- It can be used for longitudinal and transverse feedback applications in storage rings as well as for bunch-by-bunch diagnostics. The "iGp" system uses EPICS as operator interface, working in a Fedora 8 Linux environment, an 8-bit ADC. MATLAB post-processing programs are used to analyze feedback performances and beam instabilities [EPAC2006, WEPB28].
- DAFNE (LNF) has six bunch-by-bunch feedbacks currently running. On the e+/e- transverse planes there are 4 "iGp" feedback units. On the longitudinal planes the old "DSP-based" system is used.
- PEP-II (Teytelman, Fox) has built ~15 units of the "iGp" system, some of them have been planned for working as bunch-by-bunch diagnostics systems.
- KEK (Tobiyama, Obina) has built a version the "iGp" system made in Japan to be used for the B-Factory longitudinal plane and in the Photon Factory.
- ALS (Berkeley) is installing one iGp unit on the longitudinal plane.

# iGp last version (4/4/08)

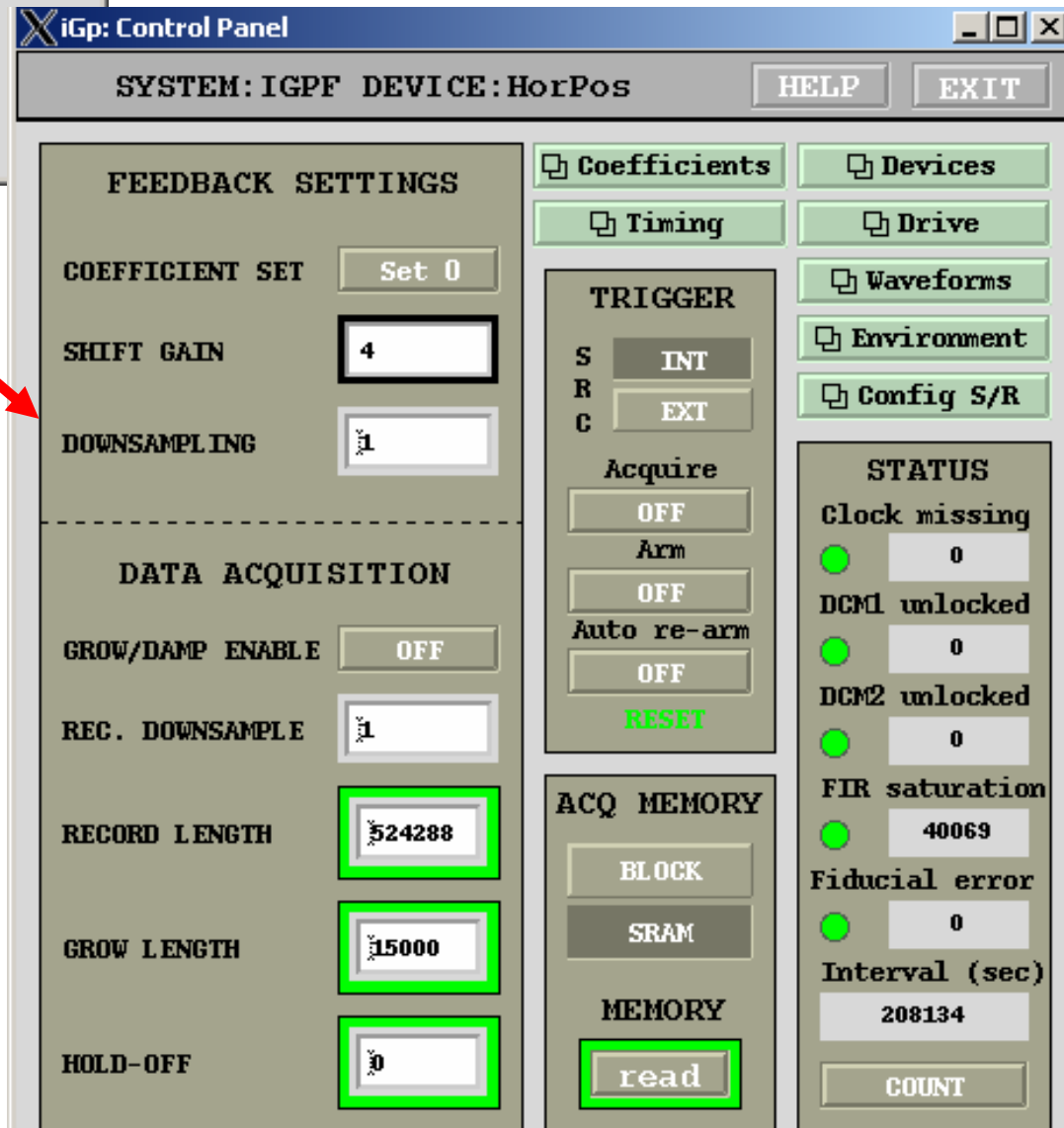
- Changes in Software and Gateware
- All iGp systems have been updated to the newest gateware (FPGA code) and software version;
- Added a powerful LINUX (Fedora 8) server in the control room to run user interface for all the six feedback systems.

# Diagnostic tools inside the feedback system

- From the Epics panels:
  - Input signal record with trigger from operator
  - grow/damp record with trigger from operator
  - Record on injection with injection trigger from the timing system
- From Matlab :
  - Store of recorded data in a time-stamped database with 2 files in matlab format
  - Post-processing analysis on the database
  - Modal analysis (mode number and grow rate)
  - Injection data analysis to study the injection kicker effects versus kicker setup and timing
  - Tune spread analysis



EPICS  
Operator  
interface



# How to build a new real time FIR filter

**XiGp: Coefficients** [System: IGPF Device: HorPos] [HELP] [EXIT]

**NEW COEFFICIENTS VECTOR**

Description

Gain=0.70;Phase=-139.0;Freq=0.10;Taps=4

[Generate]

**COEFFICIENT SET 0**

Description

Gain=0.70;Phase=-139.0;Freq=0.10;Taps=4

**COEFFICIENT SET 1**

Description

Gain=0.00;Phase=84.0;Freq=0.10;Taps=6

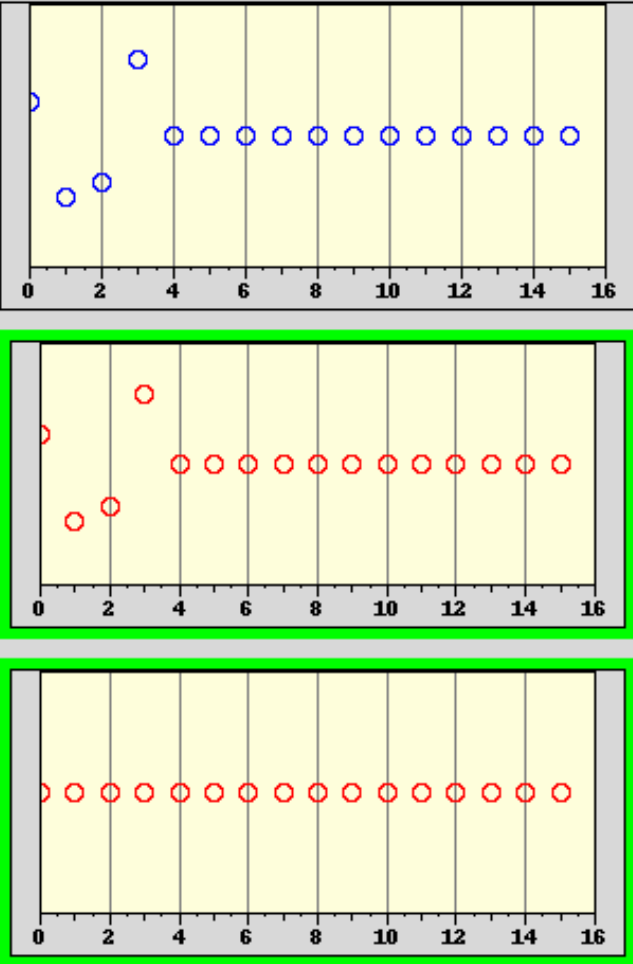
TARGET SET

Set 0

Set 1

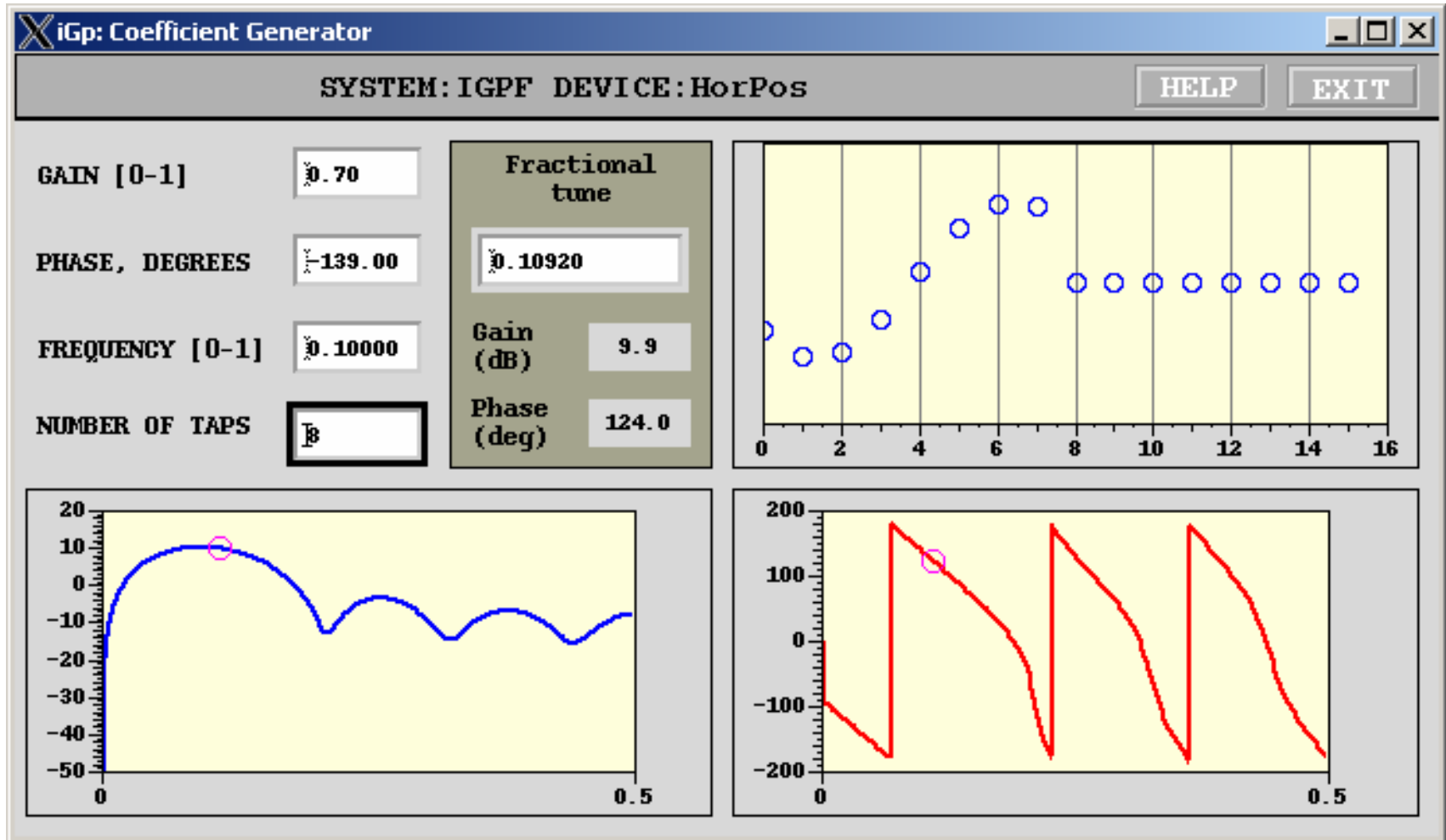
LOAD COEFFICIENTS [LOAD]

VERIFY COEFFICIENTS [VERIFY]



The top plot shows the coefficient distribution for the 'NEW COEFFICIENTS VECTOR' (4 taps). The x-axis ranges from 0 to 16, and the y-axis ranges from -0.5 to 0.5. The coefficients are represented by blue circles. The middle plot shows the coefficient distribution for 'COEFFICIENT SET 0' (4 taps). The x-axis ranges from 0 to 16, and the y-axis ranges from -0.5 to 0.5. The coefficients are represented by red circles. The bottom plot shows the coefficient distribution for 'COEFFICIENT SET 1' (6 taps). The x-axis ranges from 0 to 16, and the y-axis ranges from -0.5 to 0.5. The coefficients are represented by red circles.

# How to build a new real time FIR filter





# How to time the system

**iGp: Timing**

SYSTEM: IGPF DEVICE: HorPos

HELP EXIT

FEEDBACK TIMING		TIMING CONTROL	
ADC DELAY	150 ps	DCM RESET OFF	DCM PHASE 296
DAC DELAY	2300 ps	FID CLOCK OFFSET	820 ps
OUTPUT DELAY	56	FID SIGNAL OFFSET	750 ps
FIDUCIAL DELAY	47	DAC OFFSET	350 ps

**iGp: Device Controls**

SYSTEM: IGPF DEVICE: HorPos

HELP EXIT

MC100EP195 DELAY LINES		AD8842 DAC	
ADC (MAX104) CLOCK	15	0	0
FIDUCIAL CLOCK	97	1	0
FIDUCIAL	90	2	0
DAC (MAX5889) CLOCK	61	3	0
		4	0
		5	0
		6	0
		7	44

MAX1202 ADC

GPIO

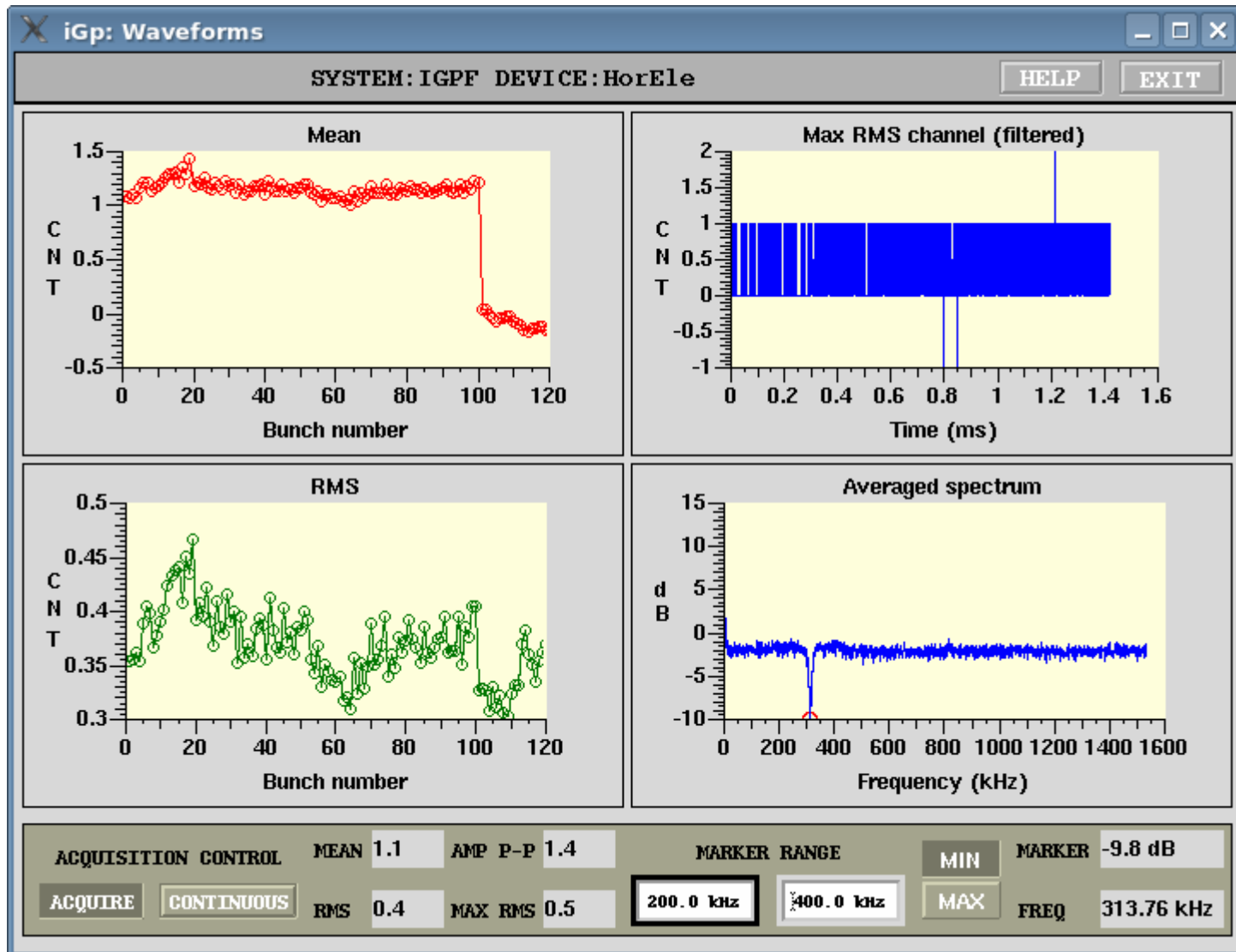
TIMING

# How to create a test pattern to drive the beam or a single specific bunch

The screenshot shows a software window titled "iGp: DAC Drive". Below the title bar is a status bar displaying "SYSTEM: IGPF" and "DEVICE: HorPos", along with "HELP" and "EXIT" buttons. The main area is titled "DRIVE PATTERN GENERATOR" and contains several controls:

- DRIVE ENABLE:** Two buttons, "Feedback" and "Drive". The "Drive" button is currently selected.
- DRIVE MODE:** Two buttons, "Bunch-by-bunch" and "Turn-by-turn". The "Turn-by-turn" button is currently selected.
- FREQUENCY:** A text input field containing "310 kHz".
- AMPLITUDE:** A text input field containing "0.100".
- WAVEFORM SELECTION:** A button labeled "SINE" with an adjacent checkbox that is currently unchecked.
- DRIVE PATTERN:** A text input field containing "1".
- ACTUAL FREQUENCY:** A read-only display showing "310.0 kHz".

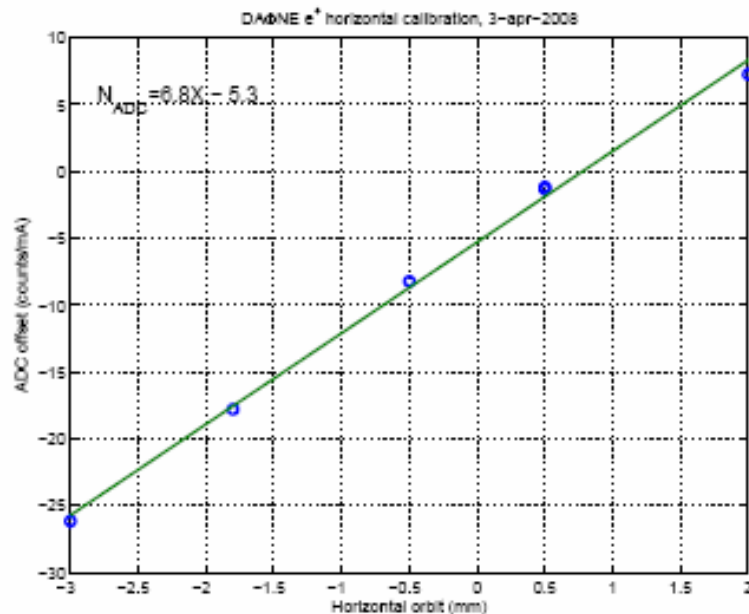
# How to monitor in real time the feedback behaviour and the beam tune



# Last changes to the system

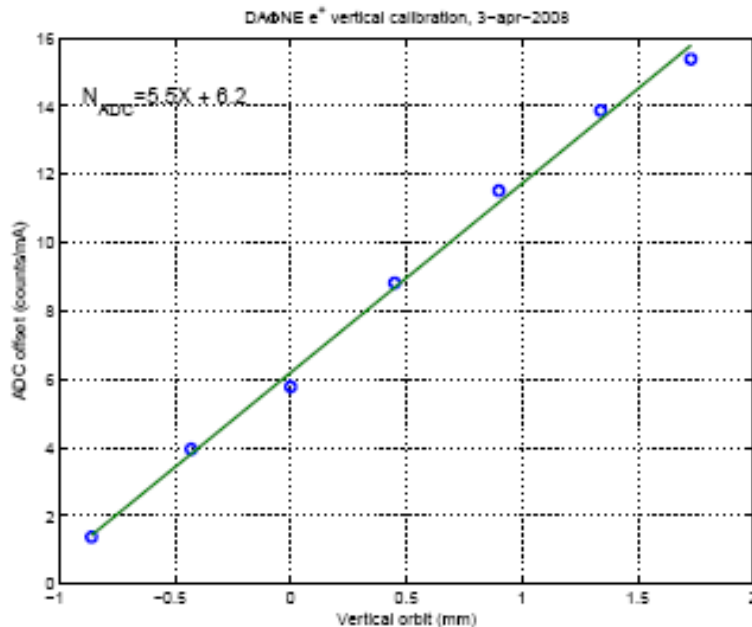
- Removed Colby delay lines from the clock signals;
- Removed manual delay lines in the output chain;
- Optimized back-end gain to match power amplifier saturation;
- Removed front-end amplifiers in all the transverse planes: now the pickup signal after passing through H9 hybrids go directly to the Analog to Digital Converter of the iGp unit. This is to have a smaller crosstalk between bunches.

# e+ horizontal system calibration



- Used orbit bumps created by Catia to calibrate the feedback input gain;
- Gain is 6.8 counts/mA/mm;
- At 10 mA per bunch ADC LSB is  $1/68 = 14.7 \mu\text{m}$ ;
- Typical residual motion at LSB/3 or  $4.9 \mu\text{m}$ .

# e+ vertical system calibration

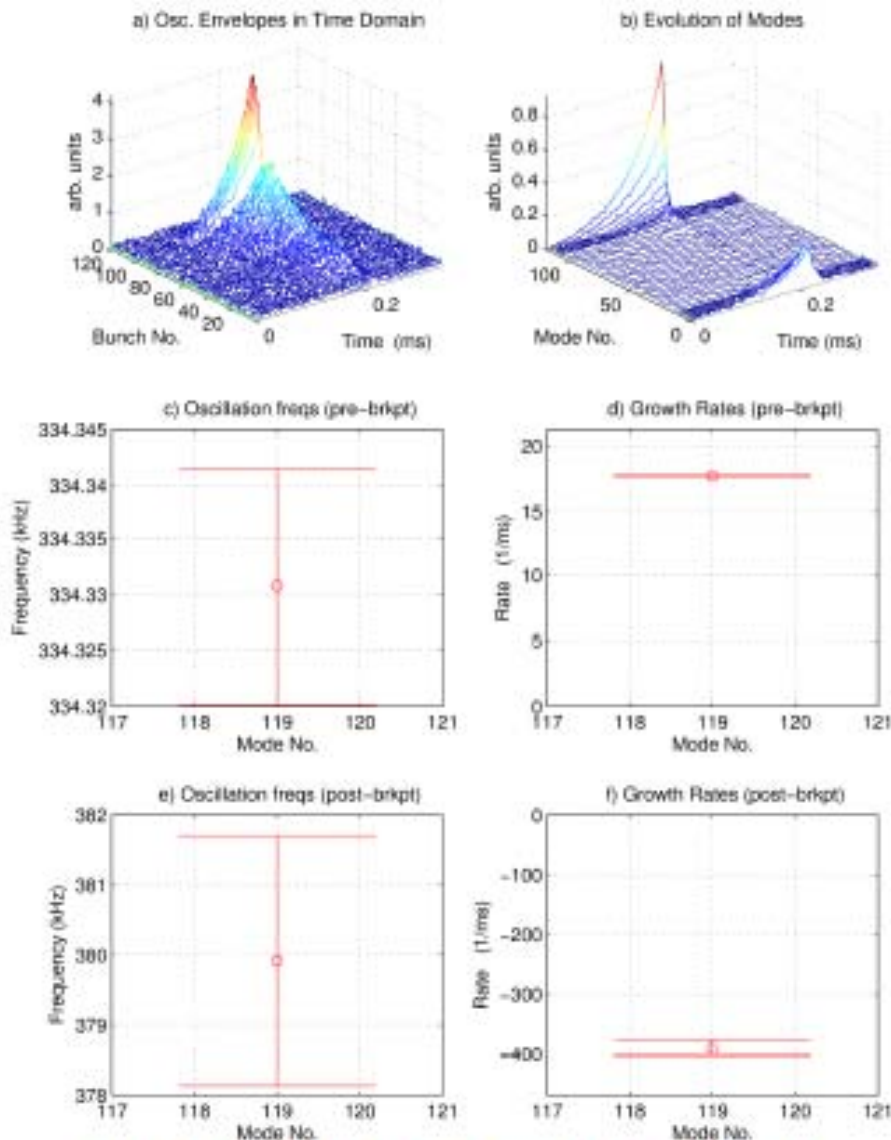


- Used orbit bumps created by Catia to calibrate the feedback input gain;
- Gain is 5.5 counts/mA/mm;
- At 10 mA per bunch ADC LSB is  $1/55 = 18 \mu\text{m}$ ;
- Typical residual motion at LSB/3 or  $6 \mu\text{m}$ .

Horizontal  
grow/damp at 355  
mA;

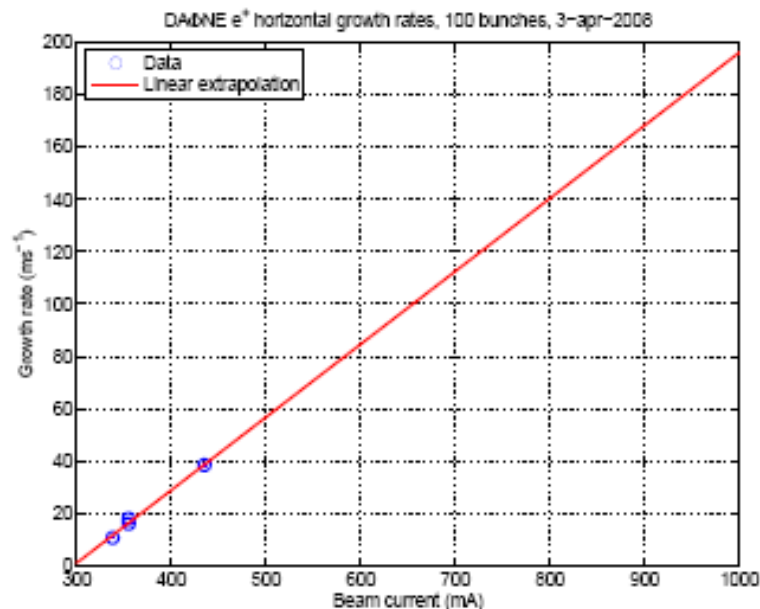
Mode -1

Extremely fast  
damping of 2.5  
microseconds rate



DAFNE E+ (ICp): apr0305214001: Io= 355mA, Damp= 1, ShiftGain= 3, Nbun= 120,  
At Fs: G1= 22.6395, G2= 0, Ph1= 144.2758, Ph2= 0, Brkpt= 659, Calib= 1.

# Horizontal Growth Rates

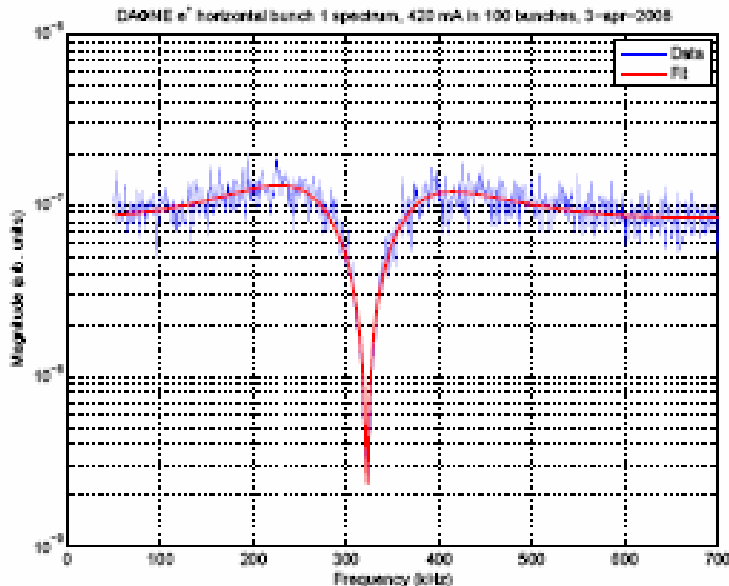


- Extrapolated from only 4 measurements;
- With 400 ms<sup>-1</sup> achievable damping should be able to support operation to 1 A and beyond;
- In practice we encountered a strong limit at 500 mA.

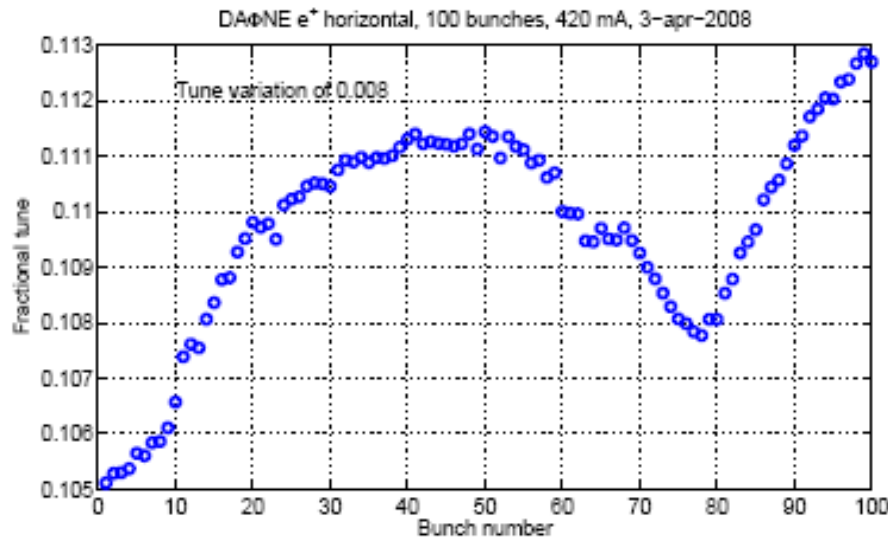


# Bunch-by-bunch Tune

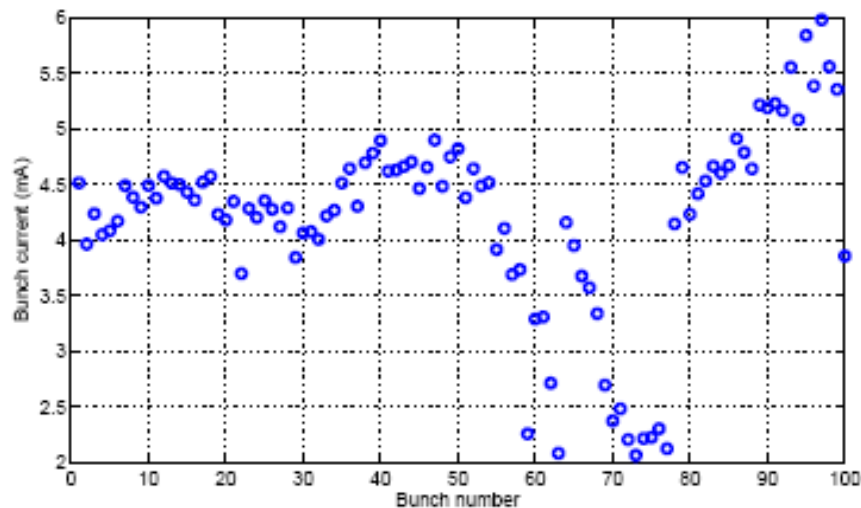
- Record beam data;
- Fit model  
beam/feedback
- response to the  
bunch spectrum;



# Bunch-by-bunch Tune

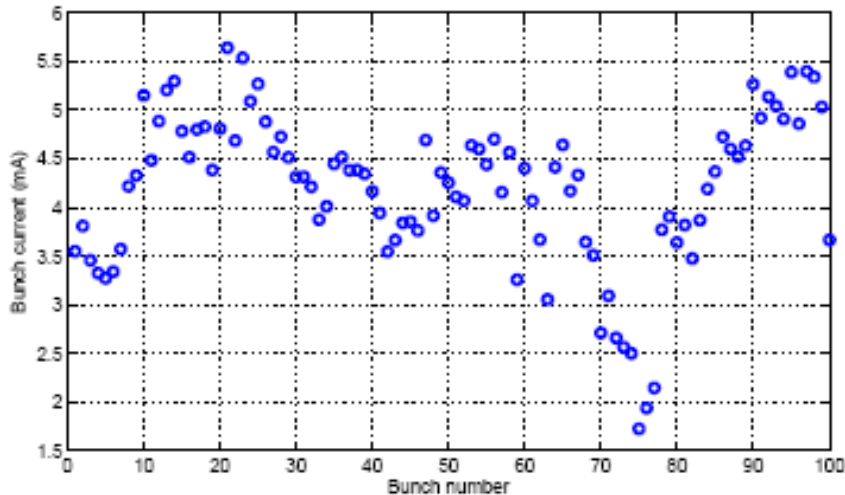
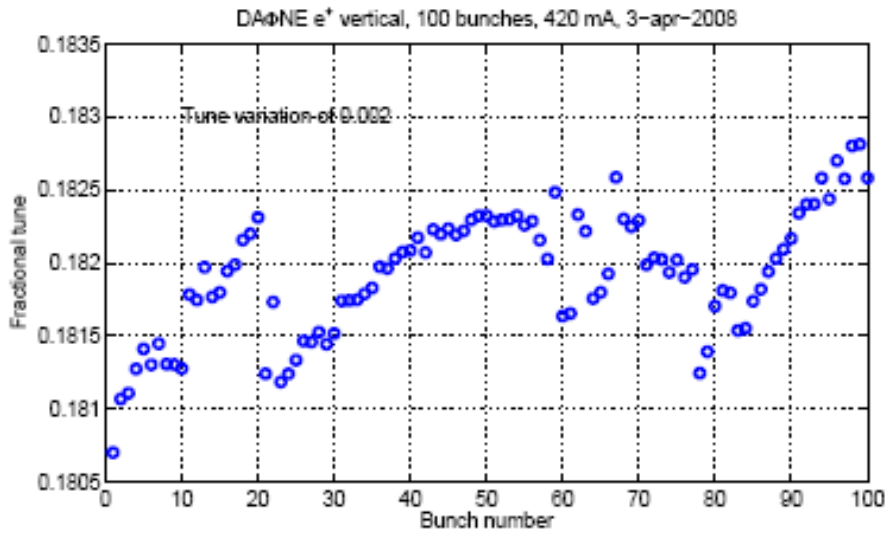


- Repeat for all filled bunches
- large tune shifts along the train in the horizontal plane;

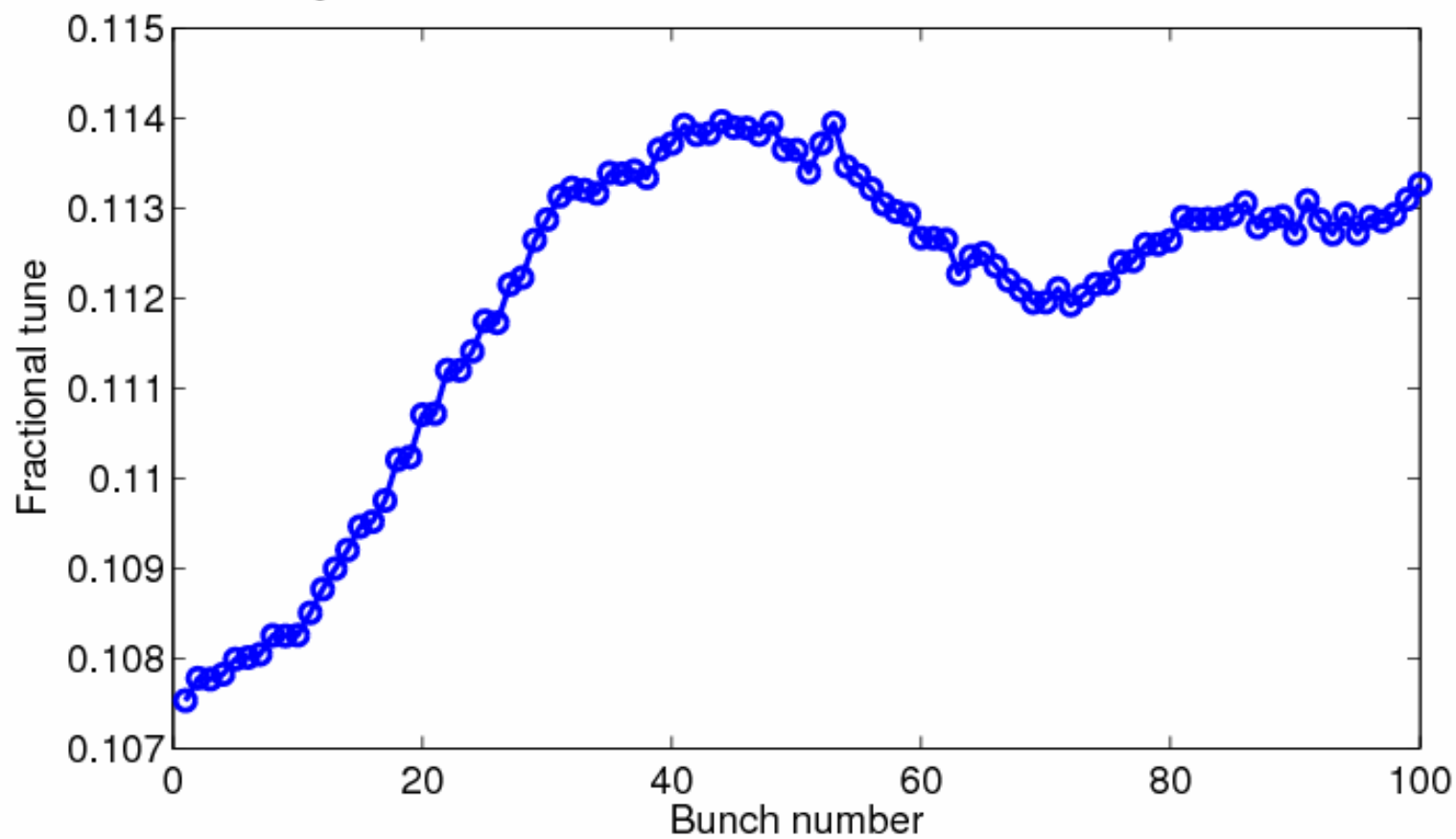


# Bunch-by-bunch Tune

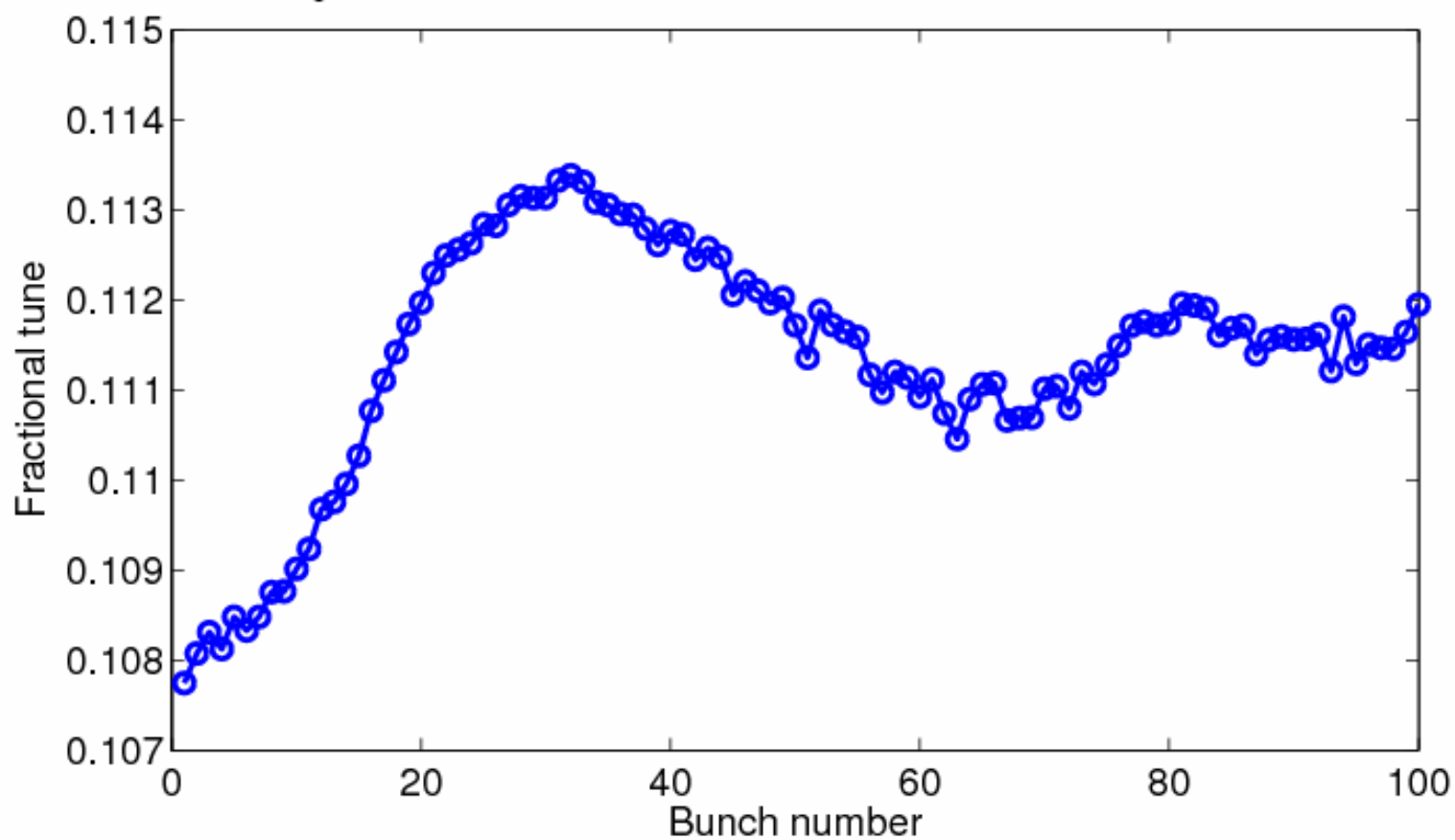
- Much smaller shifts in the vertical plane !



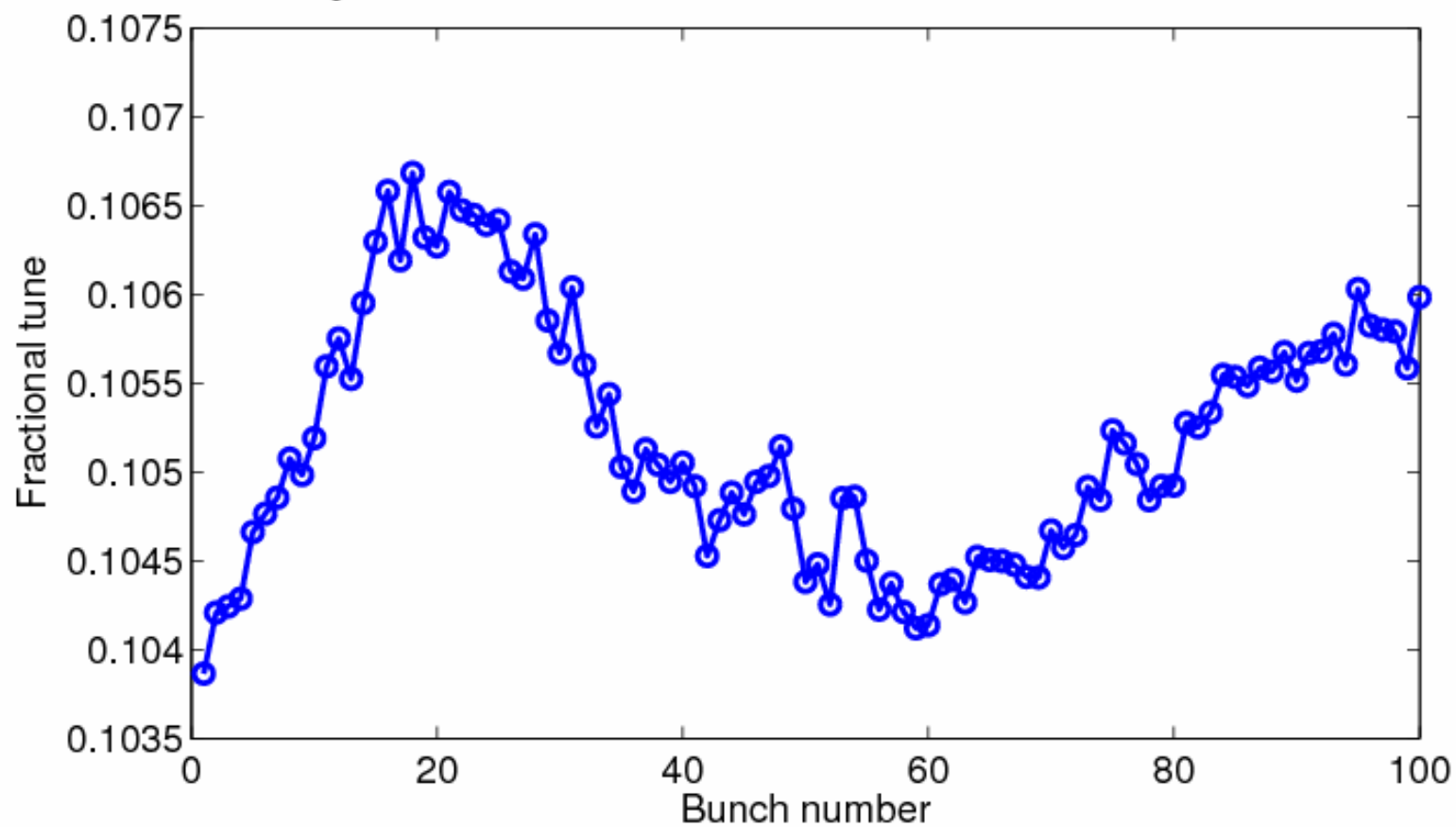
HorPos,  $I_0=415$  mA, peak-to-peak tune spread 0.0064, timestamp 143435

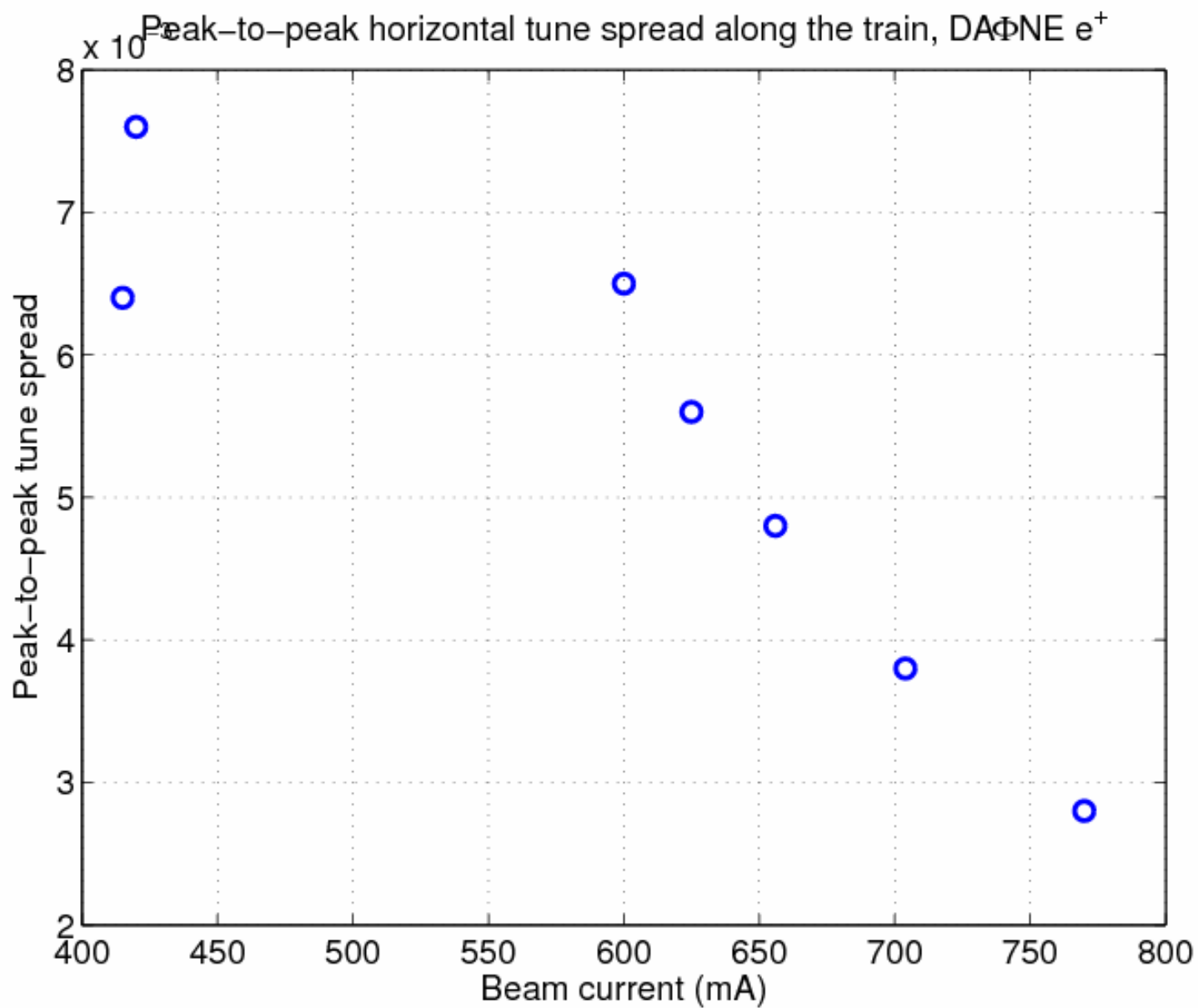


HorPos,  $I_0=625$  mA, peak-to-peak tune spread 0.0056, timestamp 142920



HorPos,  $I_0=770$  mA, peak-to-peak tune spread 0.0028, timestamp 162941





# Conclusion

- FPGA performance are growing very fast: this should be considered in the future feedback projects to add new features and more powerful capabilities
- Many interesting features are in the iGp feedback system
- Powerful diagnostics inside the system can help to understand beam current limit and feedback performance
- In DAFNE e+ horizontal plane a extremely fast mode -1 and a large tune spread limit the beam stability



Thank you for the attention!