

DIAMOND LOW POWER RF SYSTEM

C.W.Horrabin and D.M.Dykes
CLRC Daresbury Laboratory, Warrington WA4 4AD, UK

Abstract

This paper presents an overview of the low power RF system proposed to be used on the DIAMOND project. It will include detailed technical descriptions of some of the hardware building blocks and show that the use of amplitude insensitive phase detectors, originally developed at Daresbury for use on the Pohang Light Source (PLS), considerably simplifies some aspects of the design.

1 INTRODUCTION

An simplified block diagram of the proposed DIAMOND RF system is shown in Figure 1.

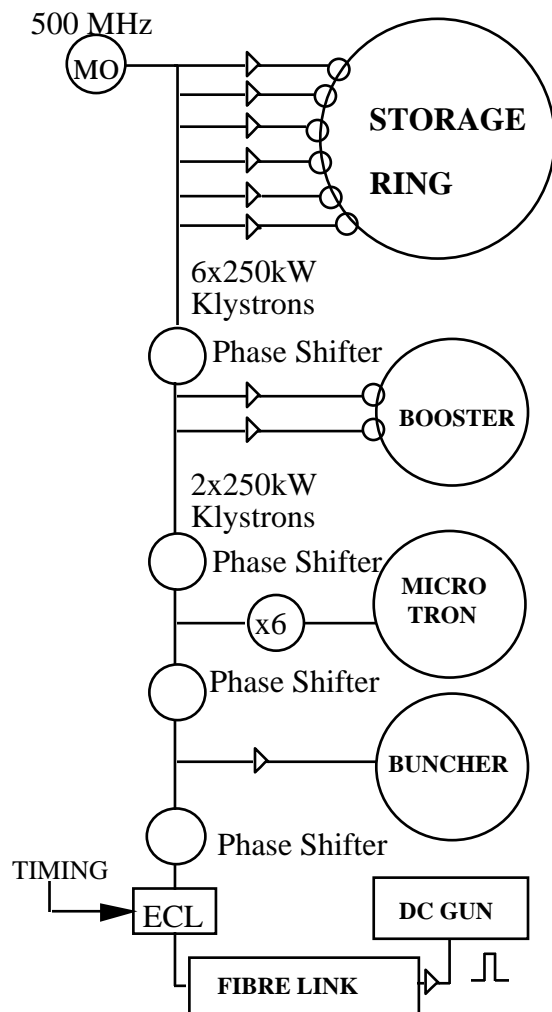


Figure 1: Block Diagram of RF System

Full energy injection from booster to storage ring will be employed. Both in the booster synchrotron and the storage ring one cavity will be powered by one 250 kW power module. This approach has some operational and design advantages and will allow the use of new crowbarless power converter technology [1]. The design of the low level RF system is also simplified as modular components already developed, by Daresbury, for the Pohang Light Source (PLS) can be applied. In particular the amplitude insensitive phase detector with a wide dynamic range [2] is used in the storage ring and booster cavity power systems and also the 500MHz buncher.

The gun will use a dc accelerating potential, with the cathode modulated with narrow pulses generated from ECL timing logic, providing different fill patterns as well as single bunch in the booster and the storage ring. Commercially designed amplifiers and fibre optic links will be used.

To help combat beam instabilities due to cavity higher order modes (HOM), by increasing the Landau damping, it will be possible to operate one of the storage ring cavities shifted by one orbit frequency, phase locked to the master oscillator.

The master oscillator uses a very low phase noise crystal oscillator mixed with the output of a Direct Digital Synthesizer (DDS) to generate the 500 MHz master oscillator frequency. The clock for this DDS chip is derived by dividing the crystal oscillator frequency. Any number of DDS chips can be synchronously mixed with the crystal oscillator to produce accurate phase locked signals or phase offsets. Usually crystal oscillators designed for low phase noise do not have good long term stability: using the DDS chips corrects for this by comparison with a precision frequency standard. In addition it enables horizontal orbit correction if necessary.

The correct phase for all components of the machine is provided by the series connection of the RF paths, separated by precision phase shifters.

2 SUBSYSTEM DESIGNS

2.1 The Master Oscillator

A block diagram of the master oscillator is shown in Figure 2.

A fifth overtone crystal is connected in a double tank U310 FET grounded gate circuit as this has superior close-in phase noise performance. The crystal oscillator is further isolated from the load impedance by a second U310 also connected in grounded gate, before further amplification and multiplication to 494 MHz. The output

is filtered and amplified to give an accurately stabilised output level of +20 dBm at 494 MHz.

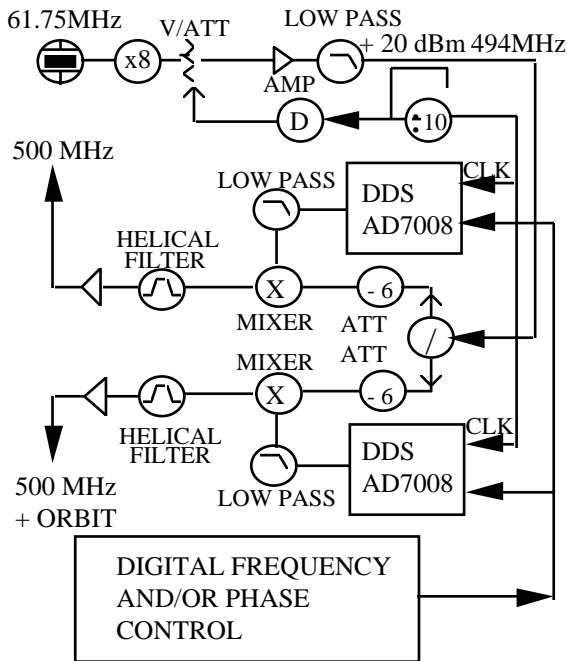


Figure 2 Master Oscillator

This signal is then split two ways in a Minicircuit PSC2-1W, the outputs are attenuated by 6 dB before connecting to the LO input of a SBL-2LH mixer. The IF input of each mixer is generated by a DDS chip whose output frequency is in the 6 to 7MHz region.

One mixer RF output is terminated by a multipole helical bandpass filter centred at 500 MHz, while the other mixer RF output is terminated in a similar filter centred nearly 900 kHz higher (i.e one orbit frequency of storage ring). This particular output may then be used with one cavity for high order mode suppression. The main 500 MHz output is amplified and further power split for general purpose use.

Initial experiments have shown that the synchronously mixed up-converters constructed as described have extremely good phase stability. Amplitude changes between 0 and 50 dB at the IF inputs cause less than 2 degree phase error at 500 MHz. This offers the possibility of using multiple mixers to give a number of independent phase outputs when using DDS chips, such as the AD7008, as a digital phase shifter. A phase offset may be added digitally to its accumulator, this could be used as an alternative to the analogue phase shifters shown in figure 1.

2.2 The Cavity Control Loop

It is intended to construct the storage ring and booster low power RF from a set of common building blocks. A typical arrangement for the control of one cavity of the storage ring RF is shown in Figure 3.

As the phase detector is amplitude insensitive, this considerably simplifies the phase control loops. As the amplitude control path is within the phase control loop, the output power and station phase are maintained regardless of the phase shifts in the amplitude controller.

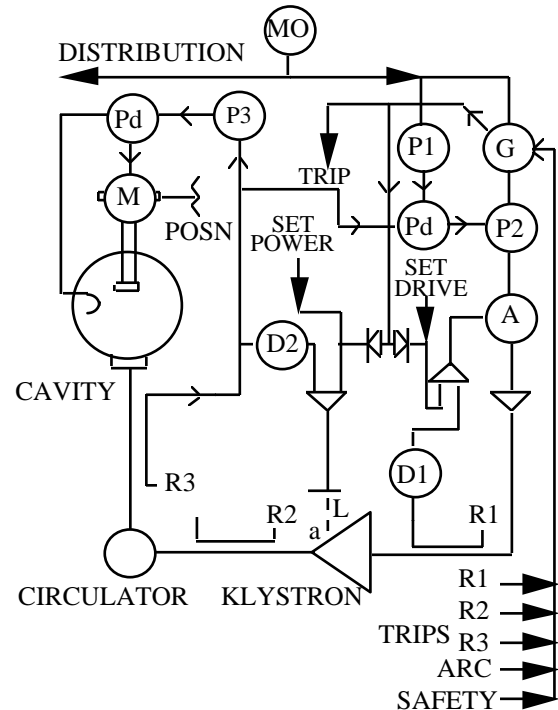


Figure 3 The Cavity Control Loop

2.2.1 Basic Operation

Most of the low level RF electronic systems for the storage ring and booster synchrotron, including the master oscillator, will be sited in a compact group of racks. The master oscillator is amplified to 10 watts, and then split in Wilkinson dividers to give 8 outputs at 1 watt, one of these outputs is further split 16 ways. Six groups of two are used in each storage ring cavity control loop. A further output goes to the booster phase shifter, and is then amplified to 1 watt for the booster RF low level control racks.

2.2.2 Cavity Control Loop Operation

Two outputs from the MO distribution are used, one goes through the set station phase shifter P1, to one input of the phase detector Pd. The other path goes through a gallium arsenide gate G and relays, to shut off the power path during fault conditions. Following this an active phase shifter P2 is modulated by the station phase control loop to maintain the forward power phase at the input to the cavity, regardless of device transit time changes (because of power level changes in the power amplification path). The klystron drive power is measured at D1 and actively set for saturated drive by the variable

attenuator A. The klystron output power is set by controlling the modulating anode voltage via the light link L.

The cavity phase angle is set by a further phase shifter P3 with a phase detector controlling the movement of the cavity tuning mechanism. In the absence of RF power the correct detune angle can be held by the tuner position potentiometer in a further motor control loop.

2.3 *Booster Synchrotron*

The Booster synchrotron cavity control loop will be similar to that described above. However as the booster acceleration will be between 5 and 10 cycles a second, the RF power will be turned down after acceleration to a few kilowatts, sufficient for the two phase detectors Pd to remain in lock. Computation of the required RF power level with magnet field during the acceleration cycle will be done by a DSP processor, and will if necessary actively control the cavity detune angle during the acceleration period.

2.4 *Injector*

The injector for the booster synchrotron has not yet been decided. However, it will be either a microtron or a linac, both available commercially and both operating at a frequency of 3 GHz. This frequency will be produced by multiplying up from the master oscillator.

2.5 *500 MHz Gun and Buncher*

It is intended to use a DC gun. Single bunch or multiple bunch patterns at the gun will be produced in a similar way to that used at the ALS [3]. In our case a single bunch from the gun of less than 300 ps is required. Commercial technology now exists to do this with 1GHz fibre links [4] and 1 GHz class A 100 watt instantaneous bandwidth amplifiers [5]. This will be confirmed experimentally: failure to achieve the results will mean that a 500MHz buncher will be required.

3 CONSTRUCTION

It is intended to build most of the low level RF system from a set of building blocks using 3U 220mm depth Eurocard system. Although the equipment supplied by Daresbury to the PLS was built in similar Eurocard modules, improved screening in the 500MHz path will be used. As a result a TNC milled lidded box measuring 25 by 96 by 96 millimetres sits immediately behind the front panel. Miniature flange mounted SMA connectors enter the box via slots in the Eurocard front panel. A 3mm wide mounting flange within the box enables a single earthplane PCB to be used with Minicircuit type components. If surface mount is used on a earthplane board, two PCB's can be placed either side of the flange forming two completely shielded compartments. Control, digital and analogue circuitry is sited on the remaining PCB area in the Eurocard module with power and control

leads entering the milled box via filtercons. Control and power connections to the module will go via the standard DIN 96-way connector. Nominal input and output RF power for a processing module is 0 dBm, although modules designed for distribution may differ from this. The intention is to build up such systems with the modules plugging in from inside the back of a 19 inch rack along with all the SMA patching cables. The result would be a clean 19 inch panel seen from the front of the rack which could carry test indication etc. The first module made to this format [6] is an amplifier 0 dBm input +30 dBm output with additional output at 0 dBm.

ACKNOWLEDGEMENTS

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REFERENCES

- [1] A Crowbarless High Voltage Power Converter for RF Klystrons, D.E.Poole et al, These Proceedings
- [2] A 500 MHz Mixer-Type Phase Detector with Wide Dynamic Range and Small Phase Error, C W Horrabin, Proceedings of Fourth European Particle Accelerator Conference pp 1975-1977.
- [3] The ALS Gun Electronic System, C.C.Lo, Lawrence Berkeley Laboratory, CA94720, USA
- [4] TESEO S.p.A. 10151 Torino (ITALY) C.so Cincinnato 228/B
- [5] Amplifier Research, 160 School House Road, Souderton PA 18964-9990, USA
- [6] Mutek Ltd, PO Box 24, Long Eaton, Nottinghamshire, UK.