Synchronizing System with Intelligence

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Abstract

A synchronizing system has been built which allows the direct injection of e- bunches from the linac into the storage ring. In order to allow a good repeatability of the fill pattern, a low jitter triggering electronics has been built. This electronics is based on the use of programmable preset counters synchronized by a clock drived from the frequency of RF. The circuits are implemented on several Euro-cards and programmed with a VMEbus. It is composed of a part of PLS control system. All trigger modules are fully controllable by the control system through VMEbus. Hence, any bunch of the storage ring is selectable and any fill pattern can also make with good repeatability.

1. Introduction

The PLS accelerator was successfully commissioned in July 1995 after the completion of the construction in 1994. It comprises two accelerators all working in concert to ultimately produce the synchrotron light. The linac as a full energy injector delivers a 2 GeV beam to the storage ring. The gun generates the electron beam with 2 A, 2 nsec long. The electron beam from the gun is accelerated to 2 GeV by 11 high-power klystrons and 10 pulse compressors located along 150 meters. It is delivered to storage ring through the beam transfer line of about 98 meters long. The flight-time of the electron beam from the gun to the end of the beam transfer line is about 830 nsec. To inject the linac bunch into the storage ring, four bump magnets and one Lambertson septum magnet are placed along the injection straight. Four bumper magnets are used to locally displace the orbit of the stored beam inward toward a septum magnet. The incoming beam from the beam transfer line is horizontally parallel with the storage ring bumped orbit and it is injected 8 degrees vertically. The Lambertson septum magnet then bends the beam -8 degrees vertically to place it on the same level as the bumped orbit of the storage ring.

Prior to the linac bunch arriving at injection point the injection bump magnet is energized to provide the appropriate magnetic field for the bumped orbit. The power supply is specified to provide a half-sine wave pulse with a base width of 4 usec. Since the magnetic field should be near it's crest when the linac bunch is arrives at the injection point, the magnet is nominally be triggered 2 usec prior to this time. This procedure is operated with 10 Hz repetition rate. The injected beam is then delivered to a predesignated bucket in the storage ring. A fundamental requirement for the successful injection is that the revolution time of the electron beam must be an integer multiple of the accelerating rf period. For the PLS this multiple is 468, which creates 468 discrete positions in the storage ring that electron beam may be within and still receive the correct acceleration from the rf to remain within the guidefields. The RF system of the storage ring is operated by the 500.082 MHz. The time between consecutive buckets passing a given point on the ring is 1.999 nsec. During physics experiment, the storage ring is normally operated in a multi-bunch mode in which some of the 468 rf buckets are consecutively filled with a 2 nsec pulse beam from the linac. It is important to inject bunched beams into the storage ring so as to satisfy the timing condition and to keep a good repeatability for fill pattern.

2. PLS Triggering System

The timing system provides a multitude of programmable trigger signals to the pulsed devices. The ultimate goal of these system is to successfully inject a electron bunch to a predesigned bucket in the storage ring. At the injection stage the gated triggers is fed to bump magnets while the gun trigger is always provided

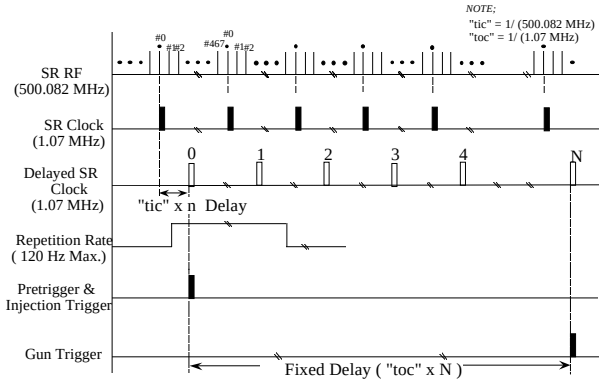

Fig.1 Timing Sequence

as a fiducial signal of the bucket selection. Basically, a trigger signal generated on the first edge of the 1.07 MHz within a gate derived from 10 Hz zero-crossing in the line frequency produces a fiducial which is superimposed on the 500.082 MHz rf signal. The timing relationship of these triggers is shown Fig.1. In these sequence all the transmission delay are neglected for simplicity. It is supposed also to be no delay for the beam from the gun to injection point (~830 nsec). There are mainly three clock signals.

- RF Clock(RFC): It has the frequency of a rf master oscillator which is 500.082 MHz. One period is equal to the time of separation between two adjacent buckets.
- Storage Ring Clock (SRC): It is a standard revolution clock of the storage ring and gives the fiducial to all the pulsed device. One period of SRC is equal to the time space of 468 rf buckets.
- Repetition Rate Clock (RRC): It decides an operating cycle to the pulsed device such as gun, klystron modulators and injection kickers.

The pretrigger must be synchronized with the RFC and the SRC and provided 102.8 usec earlier than the gun trigger for the earlier energizing of the pulsed devices. The grid trigger determines the beam timing and it is transmitted to the gun grid pulser without extra delay in order to reduce jitter of the beam with respect to the ring rf. The transfer line from the ring to the gun is about 250 m length. Since the jitter of the trigger signal to the electron beam is required to be less than +- 100 psec for the single bunch operation, we use the optical fiber and the EO/OE transmitter(ORTEL3510A) and receiver (ORTEL4510A) which has low jitter and temperature dependence. To reduce the jitter cause by the amplitude variation of output pulse, the discriminator (ORTEC935) is used after the OE receiver.

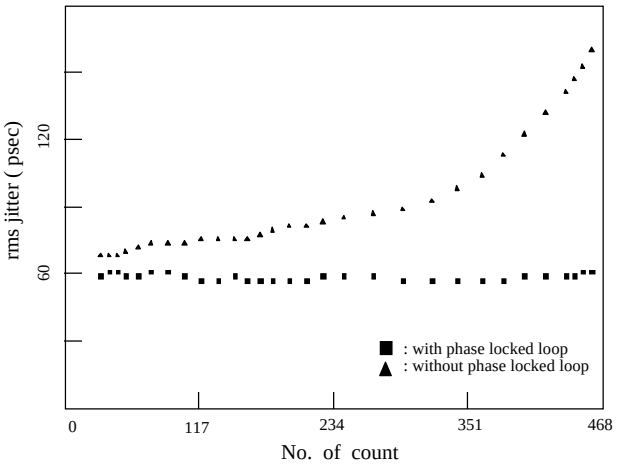

Fig.2 Jitter variation as a function of number of count with and without PLL

For the phase stability of output pulse we use a PLL at the output of trigger synchronizer. Fig.2 shows a characteristics of jitter of output signal to rf phase as function of counter clock in the two case, with and without PLL.

When an arbitrary standard SRC is defined, each bucket on the storage ring can be uniquely identified by the time displacement of integer multiple of a period of SRC. The storage ring have 468 stable rf phases(bunches) in their orbits at the interval of 2 nsec which move around the ring with a speed of the beams. If we looked at the ring by using a chopper with a repetition frequency of the SRC clock, they would seem as if stopped at fixed locations. So once a fixed standard revolution frequency was defined, each bucket can be uniquely identified by its time displacement from the standard revolution signal and can be named as #0, #1,...etc. Actually the standard revolution frequency is made dividing the rf frequency by the harmonics.

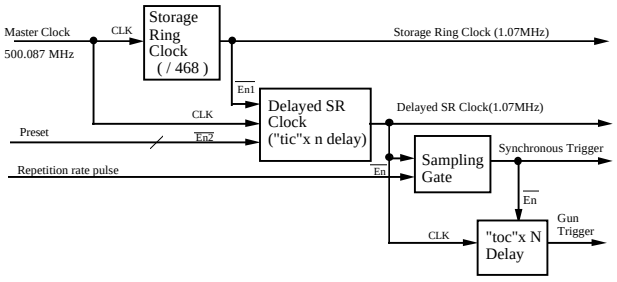

Fig.3 Bucket Selection Scheme

The injection bucket or selected bucket means the bucket which catched by the chopper situated at the injection point. The bucket selection is realized by which shifts a phase of chopper as n*pai/234. The principle of the bucket selection is shown in Fig.3. There are three stop. In the first, the SRC is obtained as dividing the RFC by the ring harmonics. The next, the SRC is delayed by a phase shifter with 2 nsec resolution. Its output is gated by a repetition rate and send to gun and kicker magnet. The selection of an arbitrary bucket is accomplished by setting the preset value corresponding to time displacement of a target bucket.

3. Description of VME Architecture

The timing requirements of the PLS control system architecture are met by a VMEbus based module which distributes the timing information to other modules within a VME crate and to the pulsed devices. The timing system is composed of five different VMEbus based modules providing all machine synchronization : a programmable line trigger, a trigger synchronizer, a fine delay module with 2 nsec resolution and 10 psec/step phase shifter, a repetition rate generator and some general purpose delay module. The circuit is equipped on the four-layer PC board for the ECL circuits which is used to eliminate ground loops cause by the signal return paths through the power feed line s and ground plate, and to provide the transmission lines with uniform characteristics. Crosstalk of adjacent signal lines can be reduced by separating the signal planes by the voltage planes. Ground lines between parallel signal lines on the same signal plan give additional protection aganist noise coupling.

3.1 Repetition Rate Generator (RRG)

This is consist of a VXI module that produces the line trigger using a programmable counter which

divides the sixty Hz line frequency by integer obtained as a combination of 60/(n1*n2) ; n1,n2 are a integer from 1 to 120. It provides the repetition rate of the pulsed devices.

3.2 Fine Delay Module (FDM)

The FDM is composed of the revolution rate generator, which is obtained by dividing the RFC by the storage ring harmonics, and the precision delay circuit. In the delay circuit, the internal synchronous oscillator generates the clock pulses synchronized by the start pulse. It is composed of a gate circuit and a delay line which determines the oscillation frequency. The input and output level of this modules is NIM level, except the RF clock pulse and TTL level output pulse through the pulse transformer. The FDM is composed of a 650 MHz preset counter, a flip-flop to start/stop counting, an AND gate to detect the coincidence with the preset data, and an up-down counter which registers the preset data on it.

3.3 Trigger Synchronizer Module (TSM)

It consists of a VXI module which produces a trigger to drive the linac gun and the SRC. The input of this module is the delayed revolution frequency (DSR) and sub-harmonic line frequency. The output of this modules, gun trigger and pretrigger have both NIM level and TTL level for the output monitoring.

3.4 Variable Delay Module (VDM)

This circuit consist in a VXI module which produces a programmable trigger for general purpose applications. The input signal are a injection pretrigger. The programmable delay is triggered from injection trigger or SRC or internal 50 MHz clock. A combination of these signals is also possible. A circuit count the SRC to obtain n*10 nsec delay (n range = 0 to 999) plus a secondary delay in range 0 to 10 usec presettable in 10 nsec step.

4. Control of Synchronizing System

The PLS control system consists of three layers of computer. The higher level is a console which are for operator interface to monitor and control the machine. The man-machine-interface on console computer display a current historical status of machine while the application processes diagnose the machine, make a feedback control, and log the monitoring information. Communication processes interface the lower level of VMEbus based data acquisition systems which are connected via Ethernet. The two lower level are sub-system control computer(SCC) and machine interface unit(MIU). The MIU is directly interfaced to the device while the SCC acts as front-end for its connected MIUs. For high flexibility and reliability of the synchronizing system, VMEbus based computer are introduced and all the timing modules are equipped on VXI crate. The timing system is compose of one SCC, called as TISCC, and some local trigger module. The TISCC is situated near by the rf station to reduce a phase jitter from the cable length. To provide remote control from the console computer at the control room, it connected with the TISCC through the Ethernet. Timing system software is composed by some OS-9 device driver and C library. The control of all injection in the machine is provided by the software resident in the timing SCC. The most important data structure used by the timing software is sharable trough the network, accessible from the control room or from the console computer to obtained the control of the injection in remote mode.

5. Reference

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