FUNDAMENTAL ARCHITECTURES OF THE DIGITAL GLOBAL ORBIT FEEDBACK SYSTEM FOR SRRC STORAGE RING

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ABSTRACT

In this paper, we would like to discuss software, hardware configurations of the Digital Global Orbit Feedback System for SRRC and how to incorporate it with the main control system. Three VME-based crates interconnected with high performance daisy-chained global reflective memory networks have been utilized to carry out the project. One crate is responsible for acquiring all Beam Position Monitoring signals into reflective memory; another is equipped with powerful Digital Signal Processor module to calculate orbit correction offsets and place results in memory networks; the other bases on calculated correction offsets in reflective memory to change orbit dynamically and communicates with the main control system for the necessity of those housekeeping works.

1 INTRODUCTION

The Synchrotron Radiation Research Center (SRRC) is a 1.3 GeV third generation light source facility which provides high brilliant VUV and soft X-ray beamlines for application users [1]. For the purpose of supplying users with stabilized beam, we have introduced the Digital Global Orbit Feedback System (DGOFS) to possibly minimize beam motions caused by various vibrations.

The main control system of SRRC is a two-level architectures with 10 Hz updating rate as shown in Figure 1 [2]. The console workstation, resides in upper level, contains the Graphic User Interface (GUI) of the DGOFS which allow operators to activate or deactivate the implemented feature. The lower level consists of Intelligent Local Controllers (ILC), which are VME-based crates actually controlling those related front end devices.

Hereinafter, we will describe software, hardware architectures and some important considerations to incorporate the DGOFS with main control system. As for the orbit feedback control algorithm, it is the main topic of another paper written by my colleagues [3].

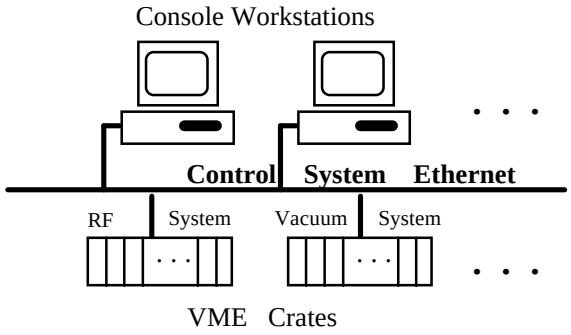

Figure 1: Control system of SRRC

2 HARDWARE CONFIGURATIONS

To implement the DGOFS, we have enhanced three existed ILCs, on the lower level of control system, with some special purpose interfaces, and rearranged Beam Position Monitor (BPM) signals, cabling layouts already connected among them.

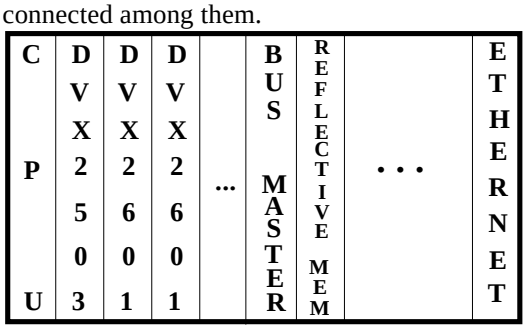

Figure 2: Layout of the first ILC

The first ILC, as shown in figure 2, is responsible for acquiring all current readings of BPMs into the control database and the DGOFS. The CPU module runs all necessary applications to fulfill 10 Hz refreshing rate of transient database and setting requests from main control system, while the BUS MASTER module has been programmed to drive DVX2503 multichannel data acquisition system. It can automatically scan all BPM analog input readings into 26.1 Mbytes/sec Fiber-Optic linked reflective memory networks through DVX2601 multiplexing interfaces. After data collection, the BUS MASTER module signals the powerful digital processing

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board, on the second ILC, to begin correcting offset calculations with respect to the existed orbit.

The second ILC, as shown in figure 3, is used to calculate correcting offsets, which will be applied on those selected correctors for reducing some vibrations of the global orbit. ADC modules are 16-bit analog input interfaces to be utilized for obtaining power supply current readings of all correctors, distributed inside the storage ring, into main control database. The DSP module is a VME-based, dedicated C40 digital signal processor board for calculating desirable corrector offsets, placing them in reflective memory networks, and signaling the third ILC to stabilize vibrations of the global orbit.

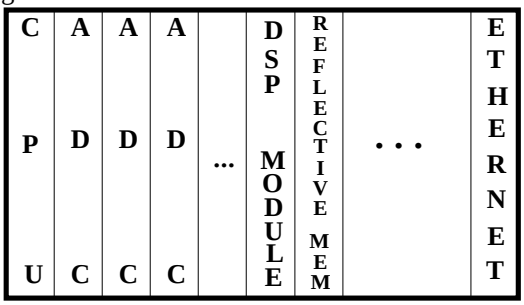

Figure 3: Layout of the second ILC

The third ILC, as shown in figure 4, actually does the orbit correction. DAC modules are 16-bit analog output interfaces for changing power supply current magnitudes of all correctors issued by the main control system or the DGOFS. Based on calculated offsets stored in reflective memory, the BUS MASTER module can drive corresponding DAC channels with respect to selected correctors to desirable currents, and modify those recorded setting values of corrector power supplies within control database.

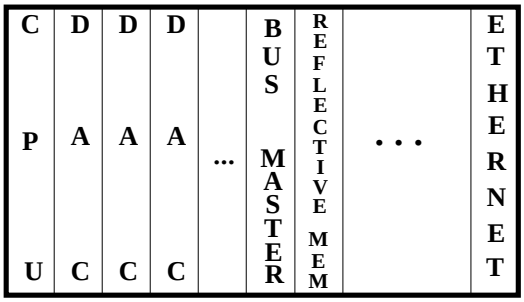

Figure 4: Layout of the third ILC

Hereinbefore, we have mentioned, lots of times, global reflective memory networks for delivering the most updated information among three selected ILC crates. Obvious advantages to utilize them lie in fast accessing time, writing data to local SRAM also being broadcasted over a high-speed fiber-optic link to other nodes, and interrupting to one or more nodes by writing to a byte register. Also the transfer of data between nodes is software transparent, hence no I/O operations are involved that releases the VMEbus for other usage.

3 SOFTWARE CONSIDERATIONS

Since the DGOFS, without dedicated VME chassis, shares resources and VME buses with main control system, we have encountered some subtle bus arbitration problems. That is the main reason why we have separated BPM, ADC, DAC modules on three different VME-based chassis threaded by high performance daisy-chained global reflective memories to minimize bus request occurrences. Also, the main control system has 10 Hz refreshing rate, which can not be ignored in any circumstance; even if the DVX2503 module has Direct Memory Access (DMA) capability, we have to abandon this sophisticated feature in order for avoiding bus contention and obtaining exact timing sequence.

The BUS MASTER module on the first ILC must be an intelligent device since it will initialize and guide the DVX2503 to acquire all BPM signals every cycle. The precise timing is a critical part of the DGOFS hence FIFO (First In First Out) data acquisition method of DVX2503 has to be adopted. Otherwise, the execution interval would varied attributing to VMEbus contention masterships of the main control system or the DGOFS, accessing latency of the resident memory modules, and internal logic of DVX2503 board. Also the BUS MASTER, on the third ILC, must have capabilities to control those DAC modules in order for setting power supplies of selected correctors.

Currently, we have provided 112 BPM-related analog input channels for orbit correction purpose and data length is less than 1K words. After DVX2503 module have finished sampling data, the BUS MASTER, on the first ILC, copies digitized data from FIFO to reflective global memory networks and sends an interrupt command across networks to signal the DSP module, on the second ILC, starting offset calculations immediately. After intensive orbit calculations, the DSP module, on the second ILC, transfers offset results and as previously informs the BUS MASTER, on the third ILC, commencing to stabilize orbit vibrations. That depicts one complete mission cycle of the DGOFS. For the moment, we have achieved approximately 600 Hz sampling frequency. Actually, the data acquisition rate of BPM signals (about 3K Hz.) is much faster than the sampling frequency. The dominating factor of slowing down the whole system performance is coming from transferring BPM digitized data to reflective memories on the VMEbus but not from offset calculation module. This is the undesirable phenomenon we will overcome and improve in the foreseeable future.

As for GUI of the DGOFS, provided to facility operators and machine researchers, is implemented to include several functions. Those are switching the DGOFS on or off, pausing or continuing the system, storing present power supply setting currents of all correctors, resetting software flow sequence of the DGOFS, remembering all BPM signal snapshot readings,

and saving machine lattice prior to turning the DGOFS on. We have testified these functions to be very helpful, and augmented capacities are reserved, undoubtedly.

4 SYSTEM PERFORMANCE

Some experimental performances of the DGOFS are described in figure 5 and 6. When the feedback system is turned on, we can observe that intentionally generated perturbations of orbits are actually stabilized to a certain extent in time varying domain.

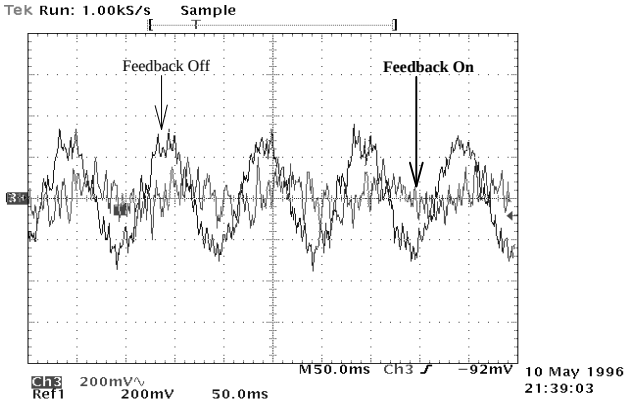

Figure 5: Comparison of orbit motion with 10 Hz perturbation

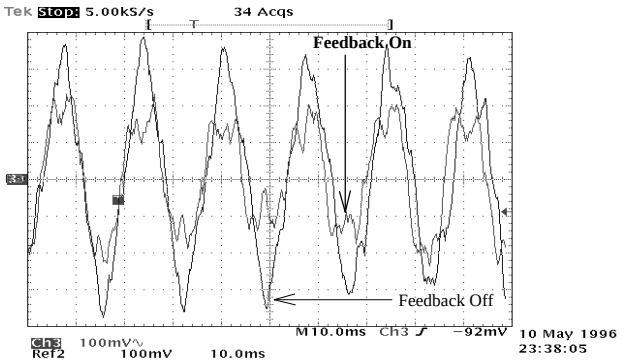

Figure 6: Comparison of orbit motion with 60 Hz perturbation

5 CONCLUSION AND PERSPECTIVE

Based on above experimental results, the DGOFS of SRRC has already accomplished parts of its expected objectives. It is an encouraged initiative which enables us to have opportunities of surveying best fitted instruments, most advanced VMEbus modules and most suitable softwares for system performance enhancing. In the future, we will manage to push the sampling frequency to 2K Hz, which is our proposed system running rate.

Since we prepare to separate the DGOFS from main control system, replace those slow VMEbus modules with much faster state-of-art versions, increase pipeline stages of data acquisitions as many as possible and minimize copy operations of online data, we ponder over that there are still lots of improvements which we can continue working on.

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REFERENCES

[1] G.J. Jan, et al., "Computer Control and Instrumentation System at SRRC", Nucl. Instr. and Meth., A 352 (1994) 33-39.

[2] C.J. Wang, Jenny Chen, J.S. Chen, G.J. Jan, "The Design Schemes of Graphic User Interface Database and Intelligent Local Controller in the SRRC Control System", Nucl. Instr. and Meth., A 352 (1994) 300-305.

[3] C.H. Kuo, et al., "First Experiments of the Digital Global Feedback in SRRC", This Proceedings.