

High Voltage, High Power Solid State Switch for Modulator Applications

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INTRODUCTION

The SLAC linac gallery is divided into 30 sectors, each housing 8 modulators. Each modulator powers a large klystron. The RF feed line to the large klystrons in each sector is driven by a unit called the RF subbooster, installed at the low energy end of each sector.

The subbooster comprises a hard tube modulator, a medium size klystron tube, their power supplies, associated low level circuitry for RF, protection, switching and timing. The subboosters are now approximately 30 years old, and in spite of some upgrades that they have received, their design remains almost original. The output stage has two vacuum tubes in parallel, with vacuum tube power supplies for electrode bias and DC power.

Faced with the need to improve the reliability and serviceability of the units and the difficulties of procuring spare parts due to the obsolescence of many of the components, we initiated a program to find low cost solutions to the problem of modernizing the gallery subboosters. As part of that program we developed a solid state switch as replacement for the modulator switch tubes.

THE APPLICATION

The existing circuit for the modulator output stage is shown in simplified form in Fig. 1. The stage is AC coupled to a Klystron tube load that takes a maximum current of 12 amps. It supplies a rectangular output pulse of adjustable amplitude (between 20 and 30 kV). The value of the coupling capacitor, C is calculated for a maximum droop in the klystron high voltage consistent with the RF phase stability [1]. The pulse pair repetition frequency is 180 Hz, maximum.

Switch design

Design parameters

Maximum voltage:	26 kV
Max. Current:	12 A
Pulse width range:	1-100 μ s
Pulse repetition Freq:	180 pulse pairs/second
Rise Time:	<100 ns

Driven by the risetime and variable pulse width requirements, we chose an FET as the switch active component. The part selected is the IRFPG50, with 1 kV VDS max and capable of carrying 6.1 amps continuous and 24 amps pulsed.

To meet the voltage specifications we decided on a stacked series design. The stack is a series of 30 stages, each stage includes a power switch element, turn-on and turn-off components, and a voltage equalization network. See Fig. 2.

The turn on circuit is a 1:1 transformer driving the FET gate through a series diode. A short (about 100 ns) turn on pulse of around 20 V on the secondary turn charges the input capacitance, leaving the FET in the on state. In the turn-off circuit a pulse (similar in amplitude and width to the turn-on pulse) is coupled to another 1:1 transformer driving directly the gate of a small FET type IRFD1Z0, that shortcircuits the power FET gate to its source, turning it off, Fig. 2. In the physical realization of the series stack each individual stage is built on a small printed circuit board, containing all the components.

Both turn-on and turn-off coupling transformers are built on small ferrite toroidal cores, mounted flat on the printed circuit board with the core hole aligned with another hole of the same size in the board. When the stage boards are stacked all the primary turns are in series, defined by a common loop of wire (60 kV silicon insulated) that threads through all the turn-on transformers and another separate loop that does the same for all the turn-off. Both loops return to the base of the switch to allow for connections and to cancel coupling with the main current path. Turn-on and turn-off pulses are about 600V, 100 ns wide pulses applied to the primary loops. The separation between the leading edges of the two pulses defines the output pulse width.

The components are all on the same side of a double sided printed circuit board, with the exception of a copper-beryllium finger contact. When the stack is assembled these fingers connect to the metal slab of the FET body of the stage underneath it, with enough pressure to secure a good contact. To allow this the power FET is mounted reversed from the usual mounting method, with the metal side (connected to the drain) upwards. The other connection to the drain, diode D2, is connected through the drain pin in the power transistor package.

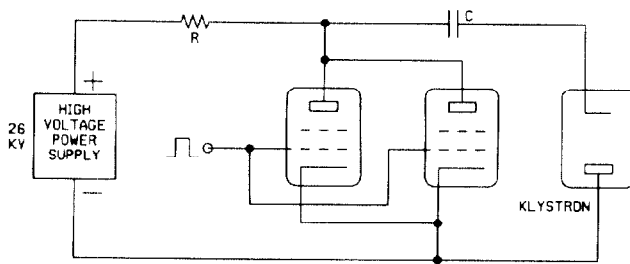


Fig 1 Simplified Modulator Schematic

The voltage equalization network, composed of D2, R3 and C1 distributes the DC off voltage evenly among all stages, absorbs overvoltage spikes, and allows for differences in the turn-on and turn-off times of the stages.

Stack assembly

After each one of the stage boards is tested, the stack is assembled by simply piling up the 30 stages separated by 6.35 mm insulating fiber washers to keep the distance between them, using two 12.7 mm fiberglass threaded rods with top and bottom nuts to hold it all together. Then the primary turns for the turn-on and turn-off circuits are threaded. A top and a bottom board are used to mechanically secure the main circuit connections. The photograph in Fig 4 show the final shape and dimensions of the stack and the stage boards.

Test setup

The test setup is rather simple, Fig. 3. We used a Glassman 30 kV max. variable high voltage power supply with a relatively large capacitor, 1 μ farad in parallel to supply the pulsed current, and two fast Pearson current transformers with a 0.25 V/Amp constant to look at the current waveforms, one at the junction between the load and the switch and another in series with the common return connection to ground (negative side). The tests were carried out with 5 k Ω , 2 k Ω and 1 k Ω loads.

Test Results

The test results can be observed in Fig 5 through 16. They are current waveforms, with a constant of 0.25 V/A. We tested the switch under a variety of anode high voltages resistive loads and pulse widths. Rise and fall times are different for the top and bottom CT's current waveforms. The top CT shows a relatively clean rise time and a slow decay. The bottom one has a large ringing in the rising phase and a clean fall time. Both the ringing and the slow fall are consistent with a 40 pF anode to ground capacitance and an estimated 1.5 μ Hy of switch assembly inductance. The top CT gives the switch inherent rise time, and the bottom the fall.

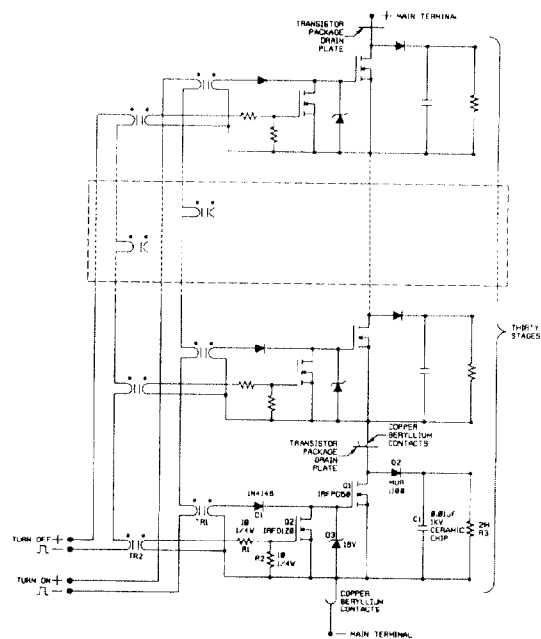


Fig 2 Switch Schematic

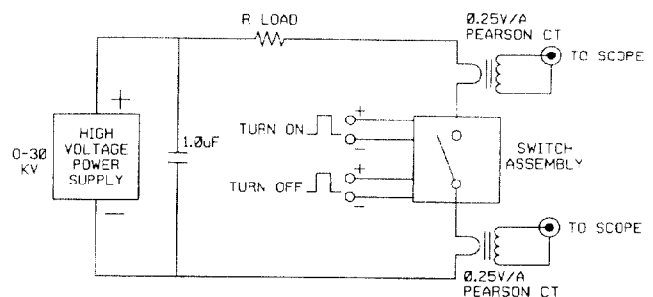


Fig 3 Test Setup Schematic

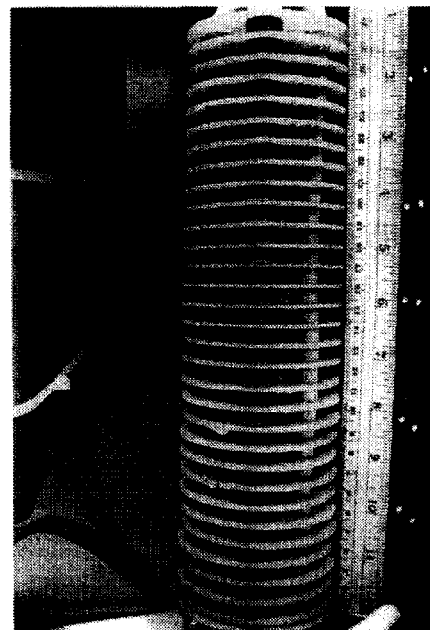


Fig 4 Switch Assembly

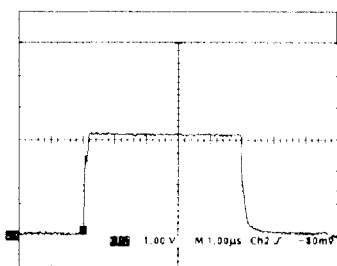


Fig 5 - 26 kV, 13A, 5 μ s, top CT

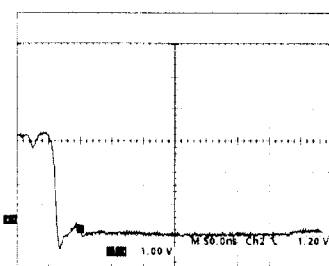


Fig 10 - Same as Fig 8, fall time

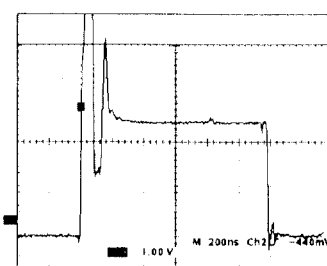


Fig 15 - Same as Fig 12, 1 μ s pulse

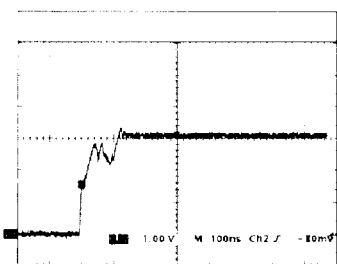


Fig 6 - Same as Fig 5, rise time

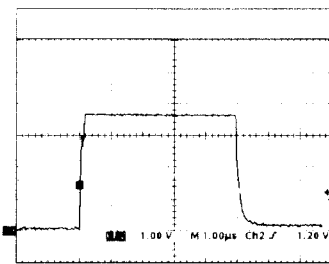


Fig 11 - 30 kV, 14.5 A, 5 μ s, top CT

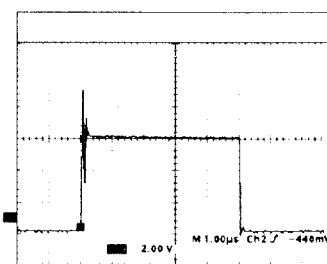


Fig 16 - 25 kV, 24 A, 5 μ s, bottom CT

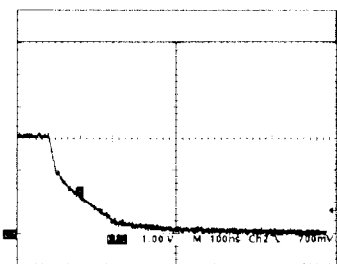


Fig 7 - Same as Fig 5, fall time

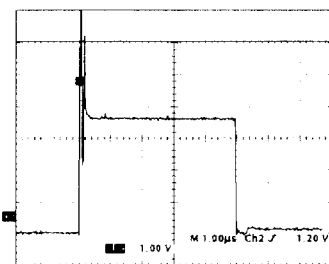


Fig 12 - Same as Fig 11, bottom CT

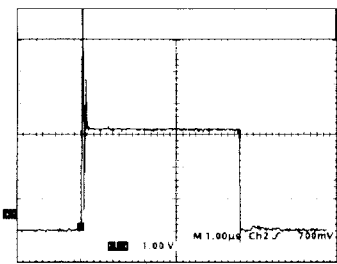


Fig 8 - Same as Fig 5, but bottom CT

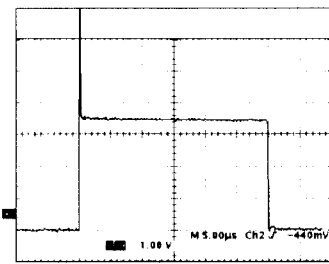


Fig 13 - Same as 11, but 30 μ s pulse

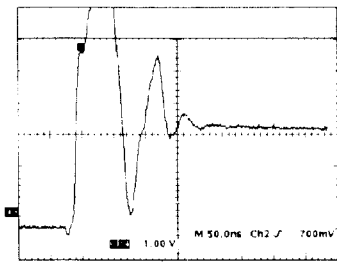


Fig 9 - Same as Fig 8, rise time

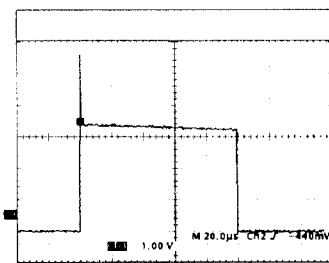


Fig 14 - Same as 11, 100 μ s pulse

The waveforms show the current response of the switch, rise and fall times, in a range up to 24 A, and from 1 μ sec to 100 μ sec pulse width. When the voltage reaches or exceeds 30 kV a level afterpulse tail appears, showing a loss in the voltage holding capacity, Fig 11 and 12.

Acknowledgements

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References

- [1] R.B.Neal, Editor. The Stanford Two Mile Accelerator, Benjamin, 1968.
- [2] A. Saab et al. Fast TEM Kicker with MOSFET Solid State Driver. Proc. of the 1991 Particle Acc. Conf. San Francisco, 1991, pp 3174.