

DIGITAL TRIGGER GENERATOR FOR A 24-PULSE SCR BRIDGE WITH CONTROLLABLE LINE-COMMUTATED FREE-WHEELING THYRISTORS*

R. Olsen
Brookhaven National Laboratory
Upton, New York, USA

Summary

The Booster of the NSLS is being upgraded with the installation of new power converters featuring full digital implementation of the feed-forward and feed-back control.[1,2,3,4] A key feature of the converters is the use of controllable free-wheeling thyristors to allow for inversion, optimal ripple performance, and optimal power factor. The implementation of the trigger generator as a state machine is described along with the derivation of the transfer function.

1. INTRODUCTION

The Booster Dipole power converter consists of a 100 volt 24-pulse rectifier to supply resistive excitation in series with a 1000 volt 24-pulse rectifier which supplies reactive excitation. Since the 1000 volt rectifier delivers zero volts during the static (injection and ejection) portion of the ramp, it is imperative that it be bypassed so that it does not contribute to output ripple, but should commutate spontaneously during the active portion of the ramp. This requirement was met by using line-commutated free-wheeling thyristors, as shown in Fig. 1b. As a consequence however, the transfer function of the rectifier requires the control of the two sets of thyristors (referred to as main and auxiliary) as a six segment piecewise continuous function shown in Fig. 6. This paper describes the derivation of the transfer function and the design of the trigger generator to provide the required trigger sequence.

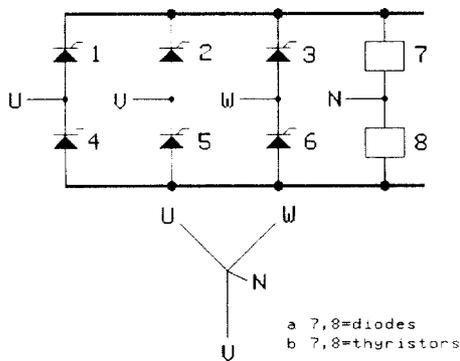


Fig. 1

2. TRANSFER FUNCTION

Although the configuration of Fig. 1a is well known, the first detailed analysis of free-wheeling thyristors was first described by Stefanovic.[5] This analysis showed that power factor and output voltage may be controlled by varying the firing angle of the main and auxiliary thyristors. Since we are interested only in optimal power factor, the transfer function was derived with this in mind. If we consider Fig. 2, we see that the phase to neutral voltage lags the phase to phase voltage by 30 degrees and that for $\alpha=0,30$ Only the main thyristors are conducting. Fig. 3 shows that for $\alpha=30,90$ both main and auxiliary thyristors are conducting, and Fig. 4 shows that for $\alpha=90,150$ only the auxiliary thyristors are conducting. The same logic holds true for inversion. For optimal power factor, we may then derive the following equations.

$$A_1 = \int_{x+60}^{x+120} \sin x \, dx$$

$$0 \leq x < 30$$

$$A_2 = \int_{x+60}^{150} \sin x \, dx + \int_{120}^{x+90} \frac{1}{\sqrt{3}} \sin x_1 \, dx_1$$

$$30 \leq x < 90$$

$$A_3 = \int_{x+30}^{180} \frac{1}{\sqrt{3}} \sin x_1 \, dx_1$$

$$90 \leq x < 150$$

$$A_4 = \int_{180}^{x+30} \frac{1}{\sqrt{3}} \sin x_1 \, dx_1$$

$$150 \leq x < 210$$

$$A_5 = \int_{210}^{240} \frac{1}{\sqrt{3}} \sin x_1 \, dx_1 + \int_{210}^x \sin x_2 \, dx_2$$

$$210 \leq x < 270$$

$$A_6 = \int_{x-60}^x \sin x_2 \, dx_2$$

$$270 \leq x < 360$$

*This work was performed under the auspices of the U.S. Dept. of Energy.

These equations are solved to give the equations.

$$A_1 = \cos x$$

$$A_2 A_3 = \frac{1}{\sqrt{3}} (\cos x + 30) + \frac{1}{\sqrt{3}}$$

$$A_4 A_5 = \frac{1}{\sqrt{3}} (\cos x - 150) - \frac{1}{\sqrt{3}}$$

$$A_6 = \cos x - 120$$

It may be observed from Fig. 4 that for $\alpha=150$, the bridge delivers zero volts but still conducts to bypass current delivered by another series power converter.

3. TRIGGER GENERATOR

It is clear from the transfer function equations that in order for the circuit to function correctly, precise control must be maintained over the triggering relationship between the main and auxiliary thyristors. To this end, a state machine was designed to perform the trigger function, with the timing functions shared between the main and auxiliary thyristor functions. This design is an improvement over a previous design [6], in that tracking of the full trigger range of 525 degrees (full rectify to full inversion) takes place using only data tables and a 0-360 degree master counter, as opposed to the original design where a second counter was synchronized to the master counter. This negates the necessity of bandwidth limiting the input data to avoid synchronization anomalies.

The design of the trigger generator is shown in Fig. 5. Data is input to two registers, one each for main and auxiliary. The transfer function equations are solved in real-time at 1440 samples per second, and the results deposited in the control registers. These registers are double buffered so that the input data is transferred to the state machine on the next sample clock.

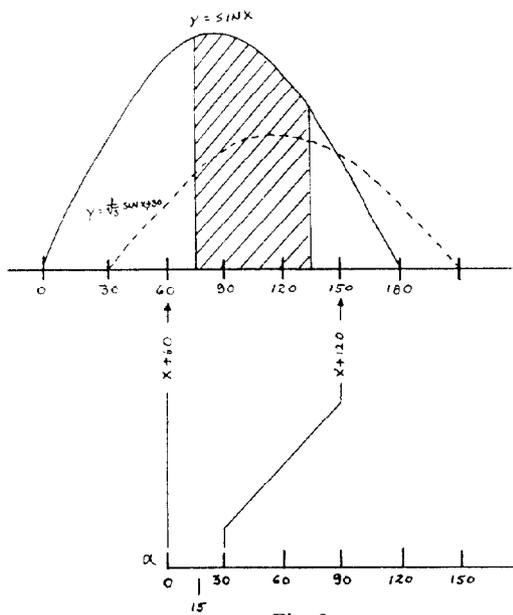


Fig. 2

The trigger generator consists of two essentially identical sub-sections with a common main counter A to track line phase and two PC (phase counters), one for each sub-system. The PC indicates the next phase to be triggered, and is controlled by two look-up tables, the PI (phase index) table and the PC control table. The input to the PI table are bits 12-16 of the A counter and bits 12-15 of the input data. The output is the phase index which

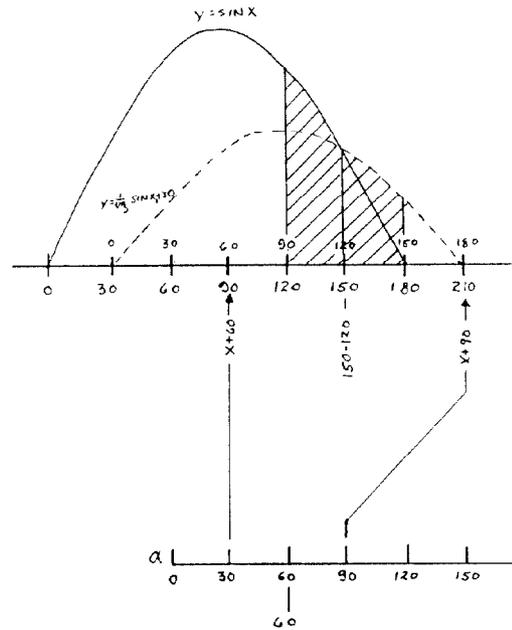


Fig. 3

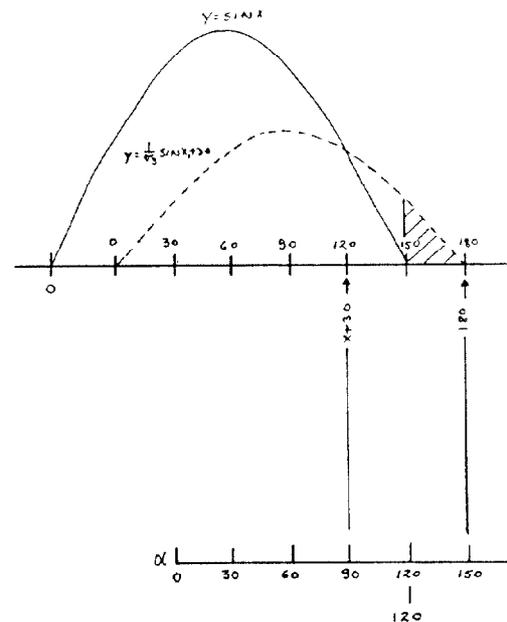


Fig. 4

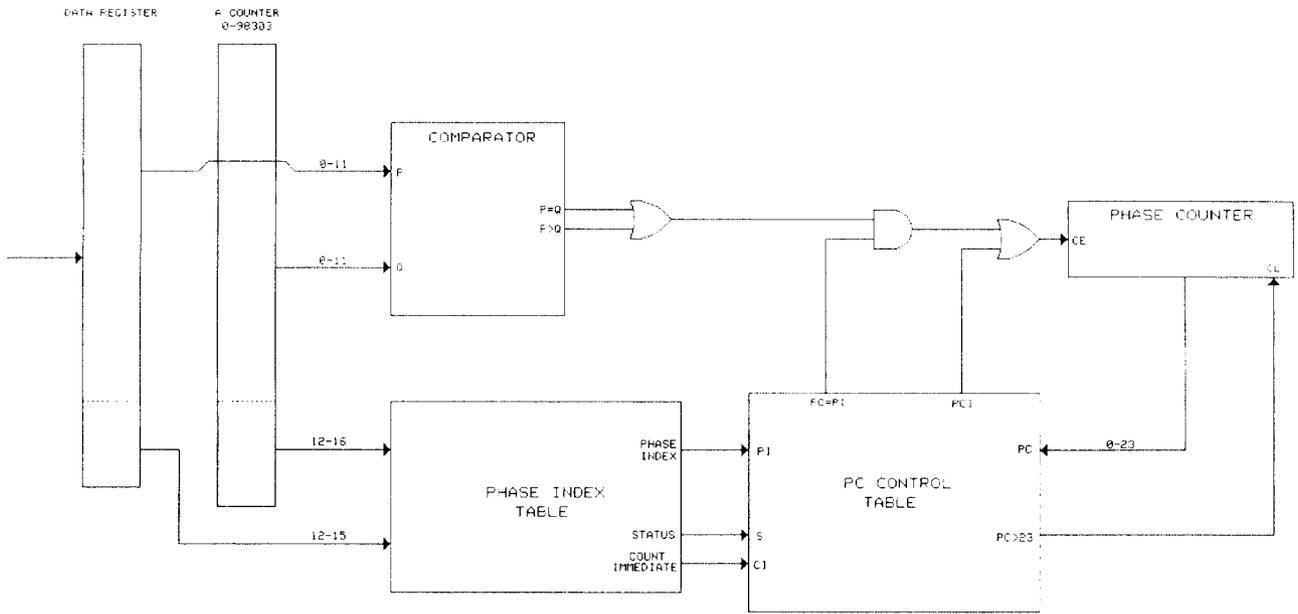


Fig. 5

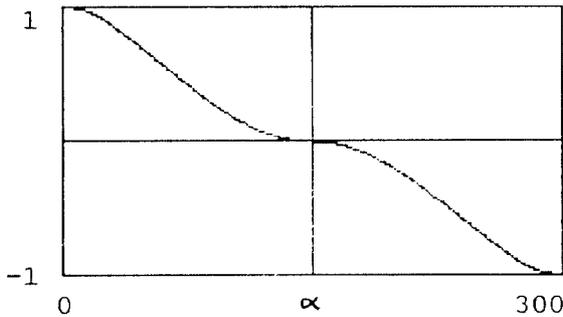


Fig. 6

indicates which phase should trigger next as defined by bits 0-11 of the trigger angle data, an (S) status bit which flags a data set of A and N and a CI (count immediate) bit which causes the PC to increment. A once per cycle pulse generated by the phase locked loop is used for synchronization.

Since $4096=15$ degrees, bits 0-11 define angles within this range while bits 12-16 define 24 blocks of 15 degrees. The outputs of the phase index table provide the inputs to the PC control table in addition to the contents of the phase counter. The outputs of the table are PCI (phase count immediate) and PC=PI. These control flags are gated with control signals derived from the low field comparator. This in turn generates a control flag which enables the increment function of the phase counter.

4. REFERENCES

- [1]J. Murray, R. Olsen, PLL Subsystem for NSLS Booster Ring Power Supply, Proceedings of the 1993 Particle Accelerator Conference, May 17-20, Washington DC, Vol 2, Page 1274.
- [2]R. Olsen, J. Dabrowski, Digital Signal Array Processor for NSLS Booster Power Supply Upgrade, Proceedings of the 1993 Particle Accelerator Conference, May 17-20, Washington DC, Vol 3, Page 1855.
- [3]R. Olsen, J. Dabrowski, Control System for NSLS Booster Power Supply Upgrade, Proceedings of the 1993 Particle Accelerator Conference, May 17-20, Washington DC, Vol 3, Page 1858.
- [4]R. Olsen, J. Dabrowski, Software Environment and Configuration for the DSP Controlled NSLS Booster Power Supplies, Proceedings of the 1993 Particle Accelerator Conference, May 17-20, Washington DC, Vol 3, Page 1861.
- [5]V.R. Stefanovic, Power Factor Improvement with a Modified Phase-Controlled Converter, IEEE Transactions on Industry Applications VOL.IA-15, NO. 2, March/April 1979.
- [6]R.E. Olsen, A High Performance Digital Triggering System for Phase Controlled Rectifiers, IEEE Transactions on Nuclear Science, Vol. NS-30, No. 4, August 1983.